EE482A Introduction to Computer Architecture
Lab 4
Robertson's Algorithm for Multiplication

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1 Introduction

The purpose of this lab is to create a VHDL design for a multiplier circuit implementing Robertson's algorithm with a state machine.

2 Equipment

Altera Quartus II software

3 Description

Design a circuit (driven by a state machine) that will implement Robertson's algorithm for two 4-bit multiplicands expressed in two's-complement format. The result will be an 8-bit number in two's-complement format.

The state machine has several functions. It

- Initializes the accumulator by clearing it.
- Initializes the multiplier register by copying the multiplier input to it.
- Initializes the multiplicand register by copying the multiplicand input to it.
- Initializes the flag register by clearing it.
- Determines the value of the flag register at each step.
- Counts (or otherwise keeps track of) the state so that it can determine whether the next partial product should be added into or subtracted from the current accumulated product and so that it can decide how to sign-extend the accululated product.

- Decides when to issue a signal indicating that the product is valid (a Done signal.) External circuits can use this signal to trigger reading the result as well as introducing a new problem to be solved.

- Shifts the two words of the product at the beginning of every cycle with appropriate sign extension.

Once you have this working properly, extend the design so that two 16-bit two's complement numbers can be multiplied to generate a 32-bit two's complement number.

If your design requires a counter, you may use any predefined counter you like. All other components must be designed by you. At your option, you may place other designs in a package.

A suggested strategy is to initialize a counter to hold the number of bits in the multiplier. The value of the counter can be an input to a state machine whose behavior will vary depending on how many bits of the multiplier have already been processed. An alternative strategy is to use a ring counter with a single one-bit in it. When that bit reaches, say, position 0, a multiplication operation is complete.

4 Lab Report

Your lab report must contain all of your fully commented VHDL source files along with simulations convincingly showing the correct operation of both versions of the circuit. Since it is infeasible to test the larger circuit for all possible combinations of inputs, test it for a representative collection of inputs. Your evidence should explore the results of multiplying by $+1$, 0, and -1, as well as by the most positive and the most negative possible numbers.

The report itself should also provide commentary on the VHDL code and the simulations so that they all can be easily understood.