

# An $R - 2R$ Digital-to-Analog Converter

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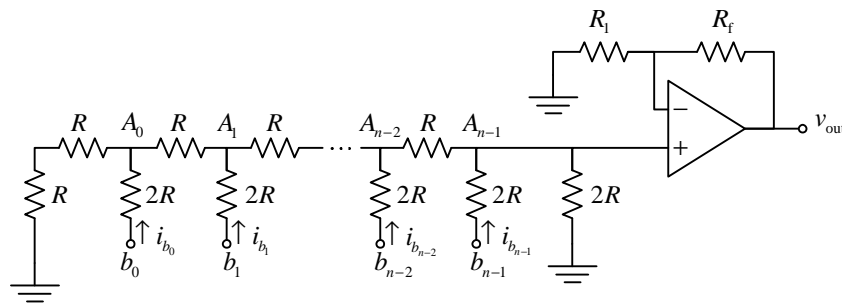
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## 1 Introduction

Many analog-to-digital converters contain a digital-to-analog converter (DAC) within them. They attempt to guess a binary value that would match their analog input and compare the output of the DAC to the unknown analog input. Using one of several possible schemes, they adjust their guess in such a manner as to minimize the difference. They then declare the guessed value to be the correct value.

Integrated circuit technology does not permit very great accuracy in choosing values of resistance. However, it does permit great accuracy in choosing resistor *ratios*. The DAC whose design is shown and analyzed below takes advantage of this characteristic of integrated circuit technology.

## 2 Analysis



In the schematic above, the inputs  $b_k$  can take on the binary values 0 or 1. The voltages  $v_k$  applied at the nodes where each binary input appears are  $v_k = b_k V_{DD}$ , where  $V_{DD}$  is the reference voltage, say, 5 V.

First treat all the inputs  $b_k$  as being grounded.

From node  $A_0$  looking left, the resistance seen is  $R + R = 2R$ .

From node  $A_0$  looking both left and down, this means that there are two resistances of value  $2R$ , one connected to ground and one connected to input  $b_0$ . Their combined resistance is  $2R \parallel 2R = R$ .

As seen from node  $A_1$ , the resistance just calculated is in series with another resistance  $R$  to the left of  $A_1$ , so their combined resistance is  $R + R = 2R$ .

From  $A_1$  looking both left and down, there are again two resistances of value  $2R$  in parallel, and their combined resistance is  $R$ .

These steps can be repeated: at every node  $A_k$ , the resistance looking to the left is  $2R$ .

A similar argument shows that the resistance looking to the right of every node  $A_k$  also is  $2R$ .

Looking both to the left and to the right of any node  $A_k$ , then, there are two resistances in parallel, both of value  $2R$ , with combined resistance  $R$ .

If we use the principle of superposition, then we can consider just one input  $b_k$  at a time, regarding all the others as 0. After analyzing just one such input, we can sum them all to find the complete response.

From the point of view of input  $b_k$ , then, the total resistance seen is that from input  $b_k$  to node  $A_k$  plus the resistance from node  $A_k$  to the left and to the right. This is a total of  $2R + R = 3R$ .

Since the resistance seen by input  $b_k$  is  $3R$ , the current leaving that input is

$$i_{b_k} = \frac{b_k V_{DD}}{3R}.$$

When this current reaches node  $A_k$ , it faces equal resistance to left and right, so it splits in half. When the half that heads to the right reaches node  $A_{k+1}$ , it sees resistance  $2R$  toward the input node for  $b_{k+1}$  and  $2R$  to the left, so the current splits in half once again.

Eventually some remnant of the original current will leave node  $A_{n-1}$ , heading to its right. This current is is

$$\frac{1}{2} i_{b_k} \left(\frac{1}{2}\right)^{n-1-k} = i_{b_k} \left(\frac{1}{2}\right)^{n-k}.$$

When this current reaches the non-inverting input of the op amp, it passes through a final resistance  $2R$  to ground, in the process producing a voltage

$$\begin{aligned} 2R i_{b_k} \left(\frac{1}{2}\right)^{n-k} &= i_{b_k} R \left(\frac{1}{2}\right)^{n-k-1} \\ &= \frac{b_k V_{DD}}{3R} R \left(\frac{1}{2}\right)^{n-k-1} \\ &= \frac{b_k V_{DD}}{3} \left(\frac{1}{2}\right)^{n-k-1}. \end{aligned}$$

We now are in a position to add up all such contributions. They appear at the non-inverting input to the op amp as

$$V_+ = \sum_{k=0}^{n-1} \frac{b_k V_{DD}}{3} \left(\frac{1}{2}\right)^{n-k-1}.$$

The op amp is part of a non-inverting amplifier configuration with gain  $1 + \frac{R_f}{R_1}$ , so the op amp's output is

$$v_{\text{out}} = \left(1 + \frac{R_f}{R_1}\right) \sum_{k=0}^{n-1} \frac{b_k V_{\text{DD}}}{3} \left(\frac{1}{2}\right)^{n-k-1}.$$

In order to simplify this sum, it is convenient to take

$$1 + \frac{R_f}{R_1} = \frac{3}{2},$$

which we can do by selecting  $R_f = R$  and  $R_1 = 2R$ . With this selection, we have

$$\begin{aligned} v_{\text{out}} &= \frac{3}{2} \sum_{k=0}^{n-1} \frac{b_k V_{\text{DD}}}{3} \left(\frac{1}{2}\right)^{n-k-1} \\ &= V_{\text{DD}} \sum_{k=0}^{n-1} b_k \left(\frac{1}{2}\right)^{n-k}. \end{aligned}$$

Now the bits  $b_{n-1}, b_{n-2}, \dots, b_2, b_1, b_0$  can be put together to form a binary fraction

$$B = 0.b_{n-1}b_{n-2} \dots b_2b_1b_0 = \sum_{k=0}^{n-1} b_k \left(\frac{1}{2}\right)^{n-k}$$

so the output of the op amp is

$$v_{\text{out}} = BV_{\text{DD}}.$$

The value of  $B$  is in the range 0 up to, but not including, 1.

The notation for  $B$  is unusual. It is really more suited to regarding the binary input to the circuit as an integer number of quantized values that to a fractional value of the reference voltage.

The notation can be altered to conform to the fractional interpretation by setting  $B = 0.b_{-1}b_{-2} \dots b_{-(n-1)}b_{-n} = \sum_{k=-1}^{-n} b_k \left(\frac{1}{2}\right)^{-k}$ . Doing so would require changing the labels on the digital inputs. The final circuit with appropriate modifications is shown in the schematic below:

