Railgun Pulse Forming Network

Problem and Design Statement

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1. INTRODUCTION

1.1 Purpose

Rail guns are the weapon of the near future for the Navy. The rail gun can greatly improve the effectiveness of surface ships by increasing the range of naval surface fire support, reducing the space needed to store propellants for ordinance, and creating a safer environment due to the reduction of propellants on board. The Department of Defense (DOD) currently desires a scaled down, but operable rail gun to display the functionality and effectiveness of this weapon.

The purpose of this project is to create a pulse forming network to power a small scale rail gun. The mechanical components of the tabletop-sized rail gun have already been assembled and only need a power supply and control algorithm to have a working system. The end result of this project should be an efficient power supply of this railgun that supplies a high current surge in a short period of time.

1.2 Background

Throughout history naval dominance has been determined by technological superiority. Naval weapons started with melee combat and then evolved to the realm of projectiles. Today's propellant based projectiles have reached limits in range and destructive capability because of size and safety constraints. The U.S. Navy is currently attempting to build a new type of projectile that is fired by electromagnetic forces through a railgun. This projectile could have an effective range on the order of 250 nautical miles (NM) while maintaining pinpoint accuracy, as opposed to current projectiles' ranges of less than 40 NM. [1]

Since railgun projectiles are fired by electromagnetic forces, there is no need to keep large stores of propellant on board as with chemical propellant-based rounds. This increases safety by reducing the amount of explosives on board. The increased speed of the electromagnetically fired projectiles eliminates the need to include explosive warheads. The kinetic energy of the round is sufficient to destroy almost any target. This increased speed also increases the effective range, which allows ships to be stationed farther from their targets.

This project was attempted in 2007 by a USNA Railgun Team. The team did not succeed in constructing a working pulse form network and railgun. They were unable to make the switches in the pulse forming network function as intended. [2] They constructed the actual railgun that we will be using with the pulse forming network that we will design and build.

1.3 Objective Tree

In Figure 1, the objective tree for the railgun illustrates the different aspects and requirements of the design.

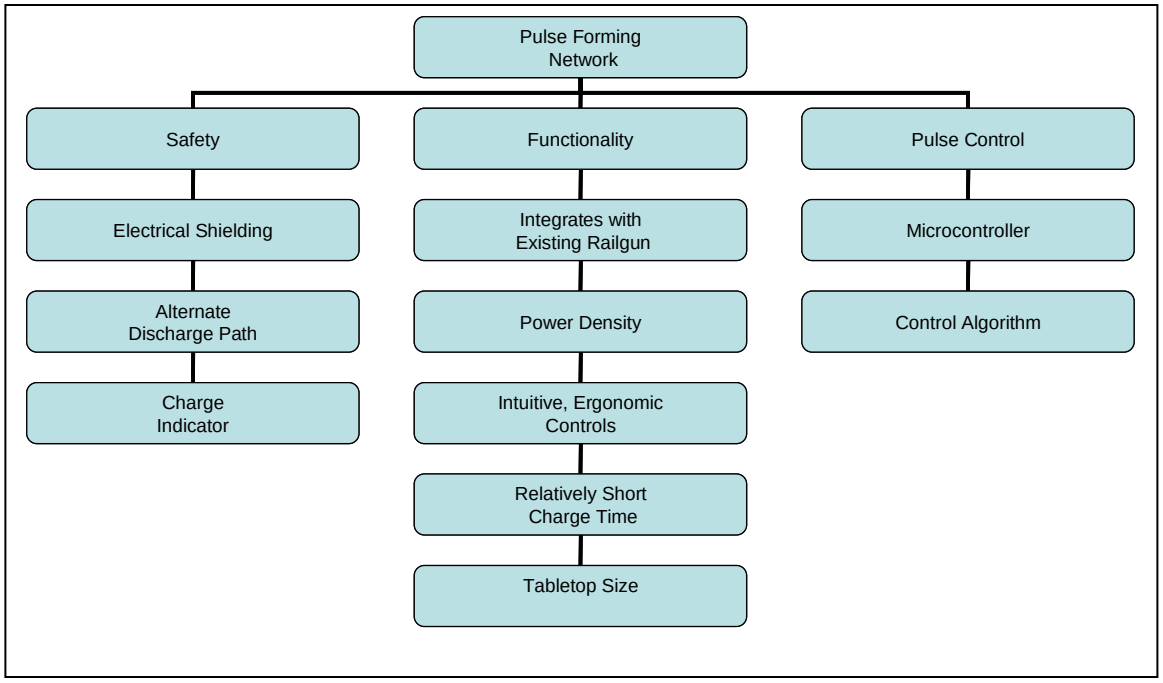

Figure 1: Objective tree for railgun pulse forming network

1.4 Requirements

Taking into account the DOD's needs, the following requirements were determined for the device:

a. *The railgun pulse forming network and railgun will fit on a tabletop (4ftX4ft).*
This is a small scale railgun for demonstration purposes. The railgun pulse forming network should be small enough to be portable and fit on a small tabletop. The railgun will be mounted on top of the pulse forming network.

b. *The railgun pulse forming network will be operated by a microcontroller using a control algorithm.*
This microcontroller allows for a compact operating system.

c. *The railgun pulse forming network charge time should be less than five minutes.*
Since this railgun will be used for demonstrations, it should not have a lengthy charge cycle.

d. *The project should not exceed $2000.*
This project is being funded by the DOD and has allotted a budget of $2000.

e. The railgun pulse forming network will deliver a current pulse of approximately 4kA lasting 5ms.
The goal is to achieve a current pulse large enough to fire a projectile with muzzle energy of 10 joules.

f. The railgun will include a safety discharge path.
A discharge path will be built that does not require firing.

g. The railgun pulse forming network will have safety features.
An indicator will notify the user when a charge is present. Components will also be shielded from contact. Further discussion on safety is discussed in section 2.3.

1.5 Scope

This project will focus on the design and construction of the pulse forming network for the pre-built railgun. The pulse forming network will be simulated, constructed with hardware, and ultimately coupled to the railgun to test firing capability. All of these steps will be performed on the Naval Academy grounds.

2. THE DESIGN

2.1 Design Overview

The railgun pulse forming network has three major components: (1) capacitor bank charging circuit, (2) a capacitor bank discharging circuit and (3) a load bank to test the network's performance,

The capacitor bank charging circuit involves connecting a source to a network of capacitors in order to create enough charge to create a current spike that will effectively fire the tabletop sized railgun. When the capacitor network is uncharged and is initially connected to the source it draws a very large current which can damage the source. To limit the initial current into the capacitor network, a current limiting capacitor charging circuit will be implemented.

The capacitor charging circuit involves a current-limiting component and switches to connect the capacitor bank to the load bank. The current limiting circuit is required to counteract the capacitor network's tendency to draw large currents when initially charging, which could damage the source. The switches in the charging circuit will merely connect the capacitor bank to the source and prevent the capacitor bank from discharging to ensure the bank can be fully charged and ready to discharge upon command. Figure 2 illustrates a simple RLC circuit that will limit the current to the capacitor bank.

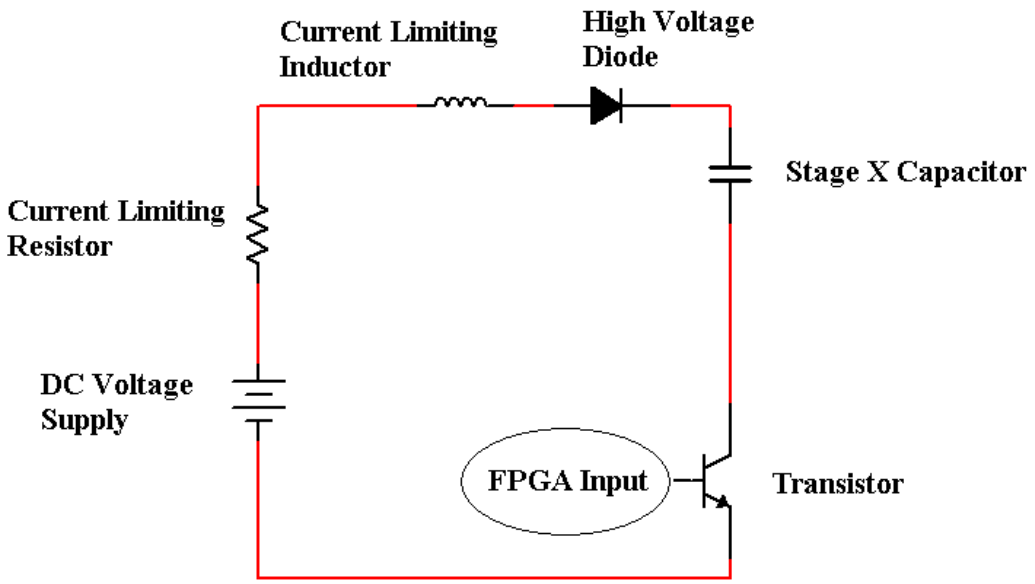

Figure 2: Current limiting charging circuit

The second component of the railgun pulse forming network is the capacitor bank discharging circuit, illustrated in Figure 3, which ensures that the network gives a satisfactory current pulse to fire a railgun. This discharging circuit will discharge capacitors in a timed sequence by closing the switches at certain times to create a net current pulse. The current output from each capacitor will have the shape of an inverted parabola, illustrated in Figure 4. However, if capacitors are charged in a timed sequence the currents can sum to form a somewhat rectangular waveform, which is ideal for the railgun.

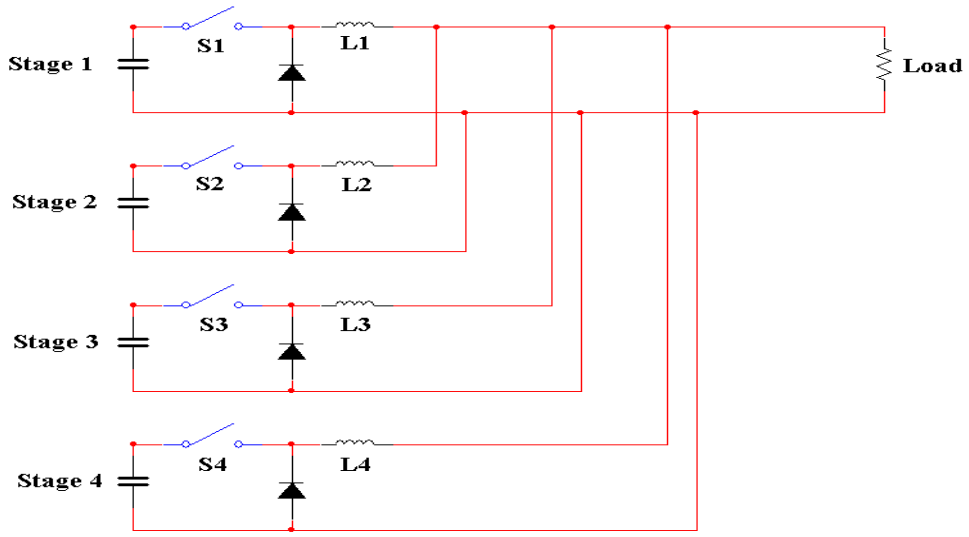

Figure 3: Capacitor bank discharging circuit

The timing component of the discharge circuit will involve a control algorithm implemented through a field programmable gate array (FPGA). This algorithm will ensure that the correct timing is used to trigger switches that will sequentially allow capacitors to discharge current creating a net rectangular current waveform. In Figure 4, the blue parabolas represent the ideal output from each capacitor bank discharge and the red quasi-rectangular waveform represents the ideal current pulse to be delivered to the railgun.

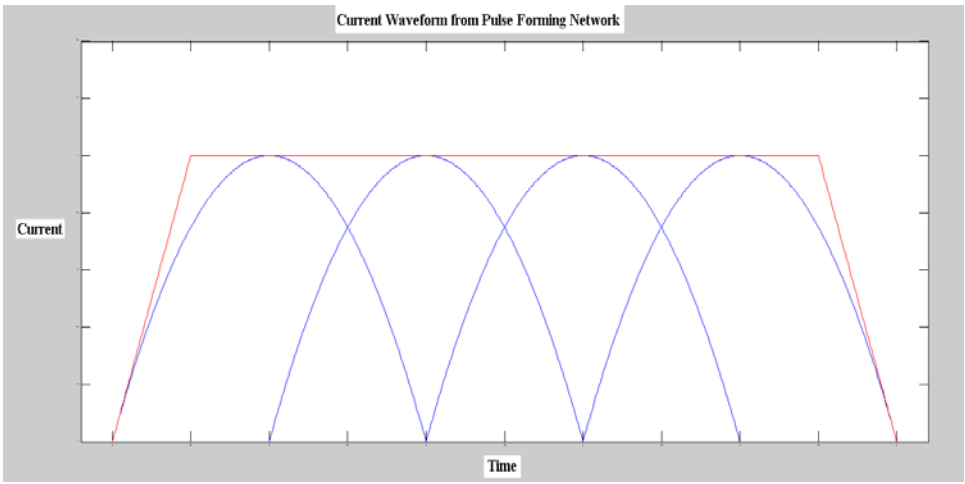

Figure 4: Ideal output waveforms. The individual current pulses are in blue and the sum is in red.

2.2 Design Details

A block diagram for the system is shown below in Figure 5a. The inputs and outputs for the FPGA controller are shown in Figure 5b.

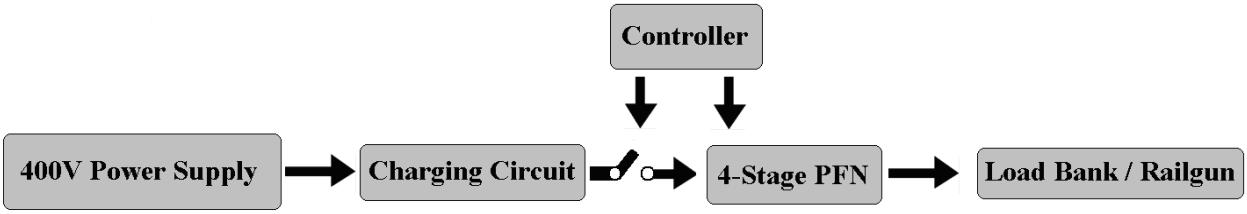

Figure 5a: Block diagram for the Railgun Pulse Forming Network.

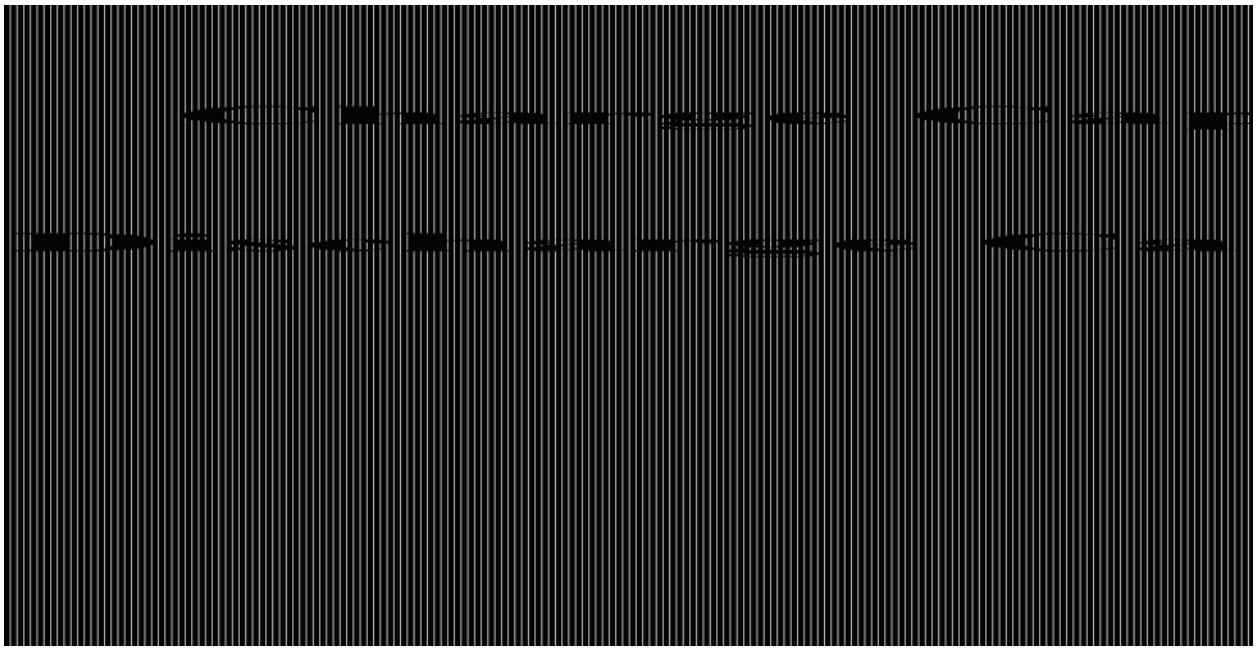

Figure 5b: Inputs and Outputs of the FPGA controller.

The morph chart in Table 1 juxtaposes the design options. The highlighted elements show which specifications were chosen for the design. The paragraphs below provide more details on each of options and the justification for the design decisions.

Means Feature/Function	1	2	3
Enclosure	PCB	Breadboard	Safety Casing
Charging Circuit	Current Limiter	Manual Current Limiting	RLC Circuit
Discharging Circuit	3-stage	4-stage	
Load Bank	Water Resistor	Resistor and Inductor	Purchased bank
Controller	FPGA	PIC	

Table 1: Morphological Chart

2.2.1 Physical Layout

We chose to mount our Pulse Forming Network Circuit onto a large board and organize it into sections. The project was set up in different sections: charging circuitry, discharging circuitry, a capacitor bank, and a load. The overall physical layout is shown below in Figure 6.

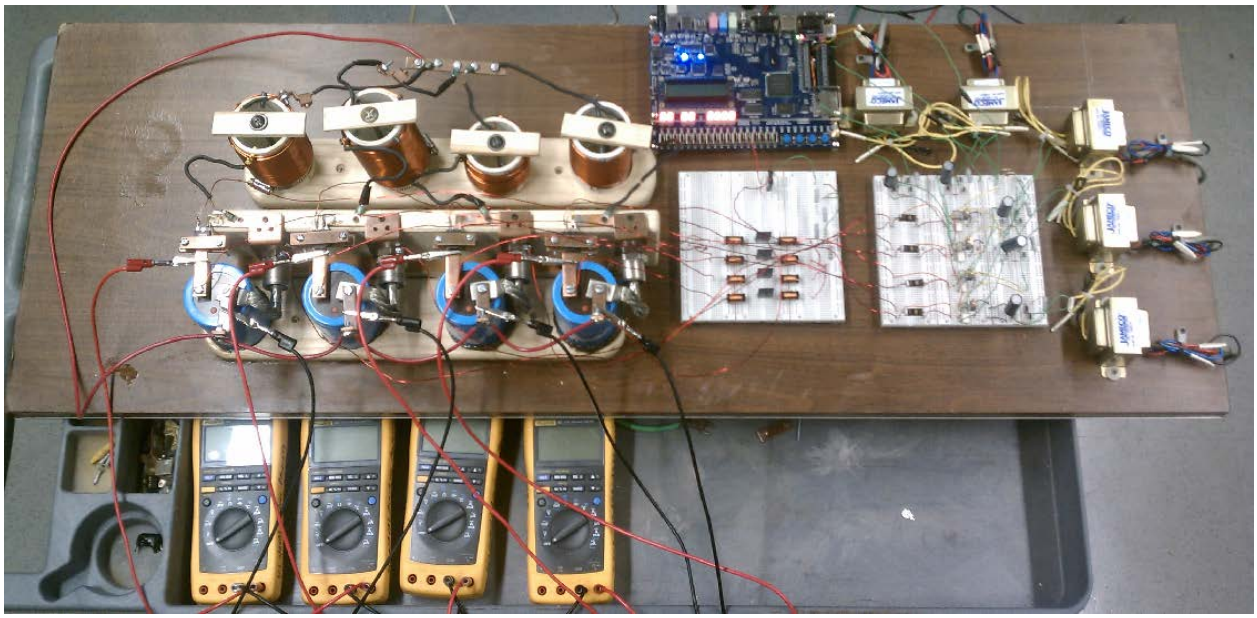

Figure 6: Overall Physical Layout

2.2.2 Charging Circuit

The capacitor charging circuit requires some method of current limiting due to the capacitor banks' high current draw when initially charging. The two options for limiting the current are a current limiting circuit and manual current limiting with the source. Manual current limiting involves incrementally increasing the power supplied to the charging circuit. This method would work, however it is not foolproof and would look unprofessional in a demonstration setting. It is also unsafe. A current limiting circuit would automatically limit the current, allowing for a simple on switch. This method is preferable, based on dependability and consistency. The circuit would mitigate the risk of damaging the source. An RLC circuit will be used because of its simplicity and low cost. The inductor will prevent a large current spike to the capacitor and the resistor will prevent the current from oscillating.

2.2.3 Discharging Circuit

The capacitor bank discharging circuit should create a net quasi-rectangular current pulse based on timed discharges of each bank. The three-phase discharging circuit and its output are shown in Figures 2 and 3. This configuration would work in creating a current pulse; however, a four phase discharging circuit would create a more rectangular current pulse.

2.2.4 Load

A load bank is required to simulate the railgun impedance when testing current levels. This impedance of the railgun can be accurately modeled as a resistance and inductance in series. A load bank with the specified resistance and inductance will safely dissipate the energy from the four stage discharging circuit. Our load bank was simply a low gauge wire that could handle on the order of 1200 amps for a 5 ms pulse.

2.2.5 Controller

The capacitor bank discharging circuit requires a controller to accurately time and coordinate the discharging of each phase of the current pulse. The controller must be easily programmable and reliable. The controllers which fit these criteria and are available for use are PICs and FPGAs. Table 2 details the advantages and disadvantages of the PICs and FPGAs.

Method	***Advantages***	***Disadvantages***
FPGA	Flexibility Processing speed Ease of Programming	Larger Topology More Expensive More Power
PIC	Less expensive Smaller	Difficult Programming Easily overloaded

Table 2: Controller selection considerations

3 SAFETY

Safety is paramount in this project, as the voltages and currents in the pulse forming network will be high enough to cause serious injury or even death. To mitigate this risk, a few safety precautions will be enacted. There will be at least two members of our project team working at all times (one that is able to shut off power if needed), and we will use good laboratory practices and common sense when operating the high voltage equipment. The pulse forming network will also have some inherent safety features. The pulse forming network will have an alternative capacitor discharging circuit so that the capacitor bank can safely discharge without firing the railgun, an indicator that will alert the user that the capacitor bank is charged or charging, and the network will have a non-conducting, but still removable, outer covering to prevent accidental injury by touching the components. The team will also prepare a safety plan including standard operating procedures for testing. Testing of the high power design will require faculty supervision.

4 METHOD

4.1 Current Limiting Capacitor Charging Circuit Design and Construction

The first step in creating the pulse forming network was to create a way to safely control the charging of the capacitor bank. If the capacitor bank is simply linked to a power source, it would cause a large surge of current, which could ultimately damage the source. To mitigate this problem, a current limiting resistor with a value of 2240 ohms and an inductor with a value of 940 micro-Henries were placed in series with each capacitor. This effectively protected the circuit and the source and caused the charging time to be approximately 90 seconds. In order to decrease the charging time, the resistance would need to be lowered. The opposite could be achieved by increasing the resistance. This circuit worked well, however, without a signal from the DE 2 Board to the transistor in the circuit the capacitor bank could not be charged. This feature was added as a safety precaution. Figure 7 below shows the Current Limiting Capacitor Charging Circuit.

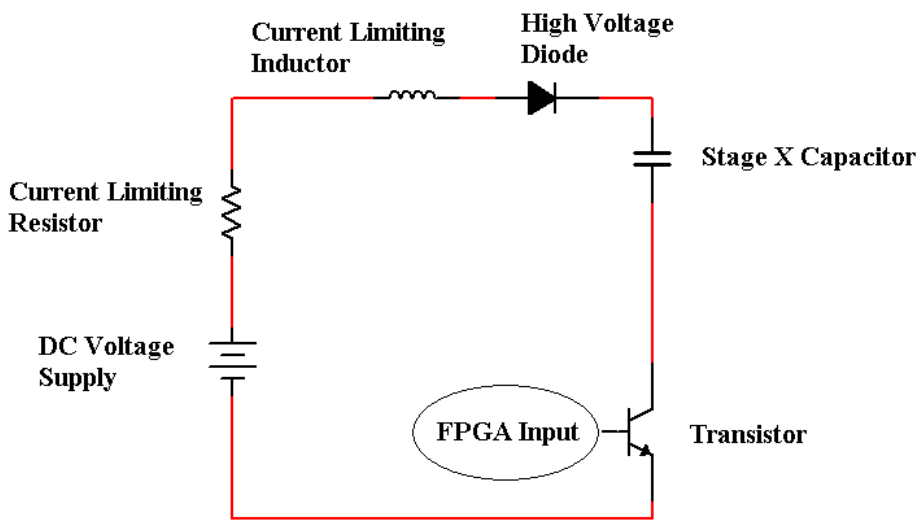

Figure 7: Current Limiting Capacitor Charging Circuit

4.2 Four Stage Pulse Forming Network

The next major circuit needed to create the pulse was the four stage pulse forming network. While four stages were adequate, adding more stages would have resulted in a better pulse waveform. The pulse forming network was relatively simple. When the switch in series with the capacitor was closed, it would discharge through an inductance, which would control the ramp-up and decay times in order to shape the waveform. After passing through the inductor, it discharged through the simulated railgun load. The diode shown in the circuit acts as a path for the current(other than through the capacitor) when it is discharging through the load. The Four Stage Pulse Forming Network circuit is shown below in Figure 8.

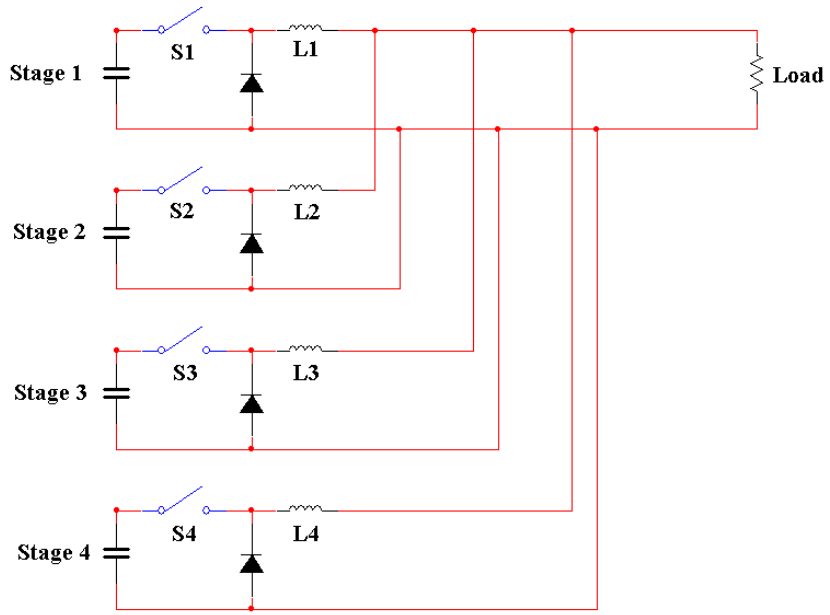

Figure 8: Four Stage Pulse Forming Network

4.3 Switching Circuitry

The switches to discharge each stage of the pulse forming network were SCR's rated at a peak surge current of 1400A. They required a gate current of 100mA or greater in order to conduct. The SCR's required a high side driver in order to turn on. This was accomplished using an optocoupler with a floating supply. Each optocoupler required an input current of at least 7mA to turn on. Each optocoupler has the ability to source up to 1.5A. The FPGA that was used cannot source 7mA of current, so the FPGA was used to turn on a smaller transistor, which then allowed enough current to flow into the optocoupler in order to turn on and activate the SCR. The switching circuitry for one phase is illustrated in Figure 9.

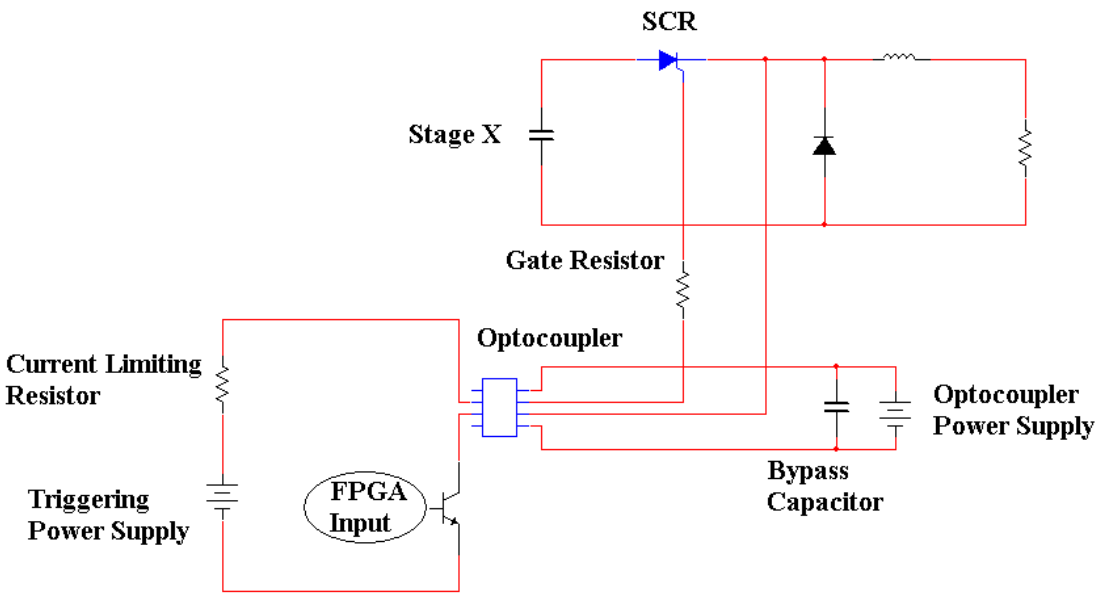

Figure 9: One Phase of Switching Circuitry

4.4 Floating Supplies

Floating supplies were needed because each source required its own ground. This was accomplished with a transformer. Power was taken from a wall outlet and fed into a transformer where the voltage was stepped down and then converted to DC. Figure 10 illustrates the H-Bridge design.

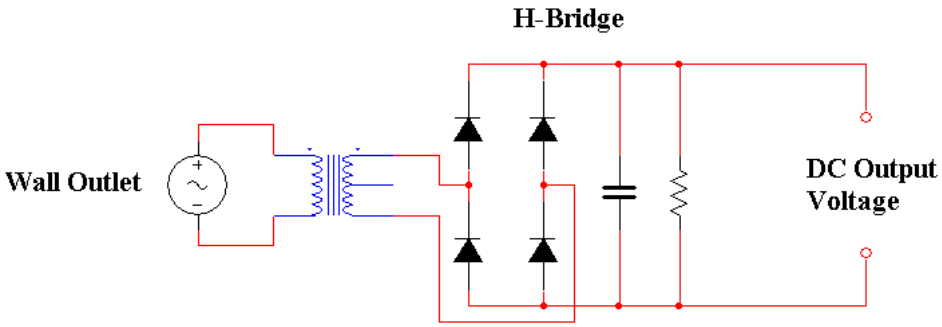

Figure 10: AC to DC H-Bridge Converter

These floating supplies were then incorporated into the switching circuitry to power the optocouplers and transistors. One complete phase of the pulse forming network can be seen in Figure 11. This includes the charging circuitry.

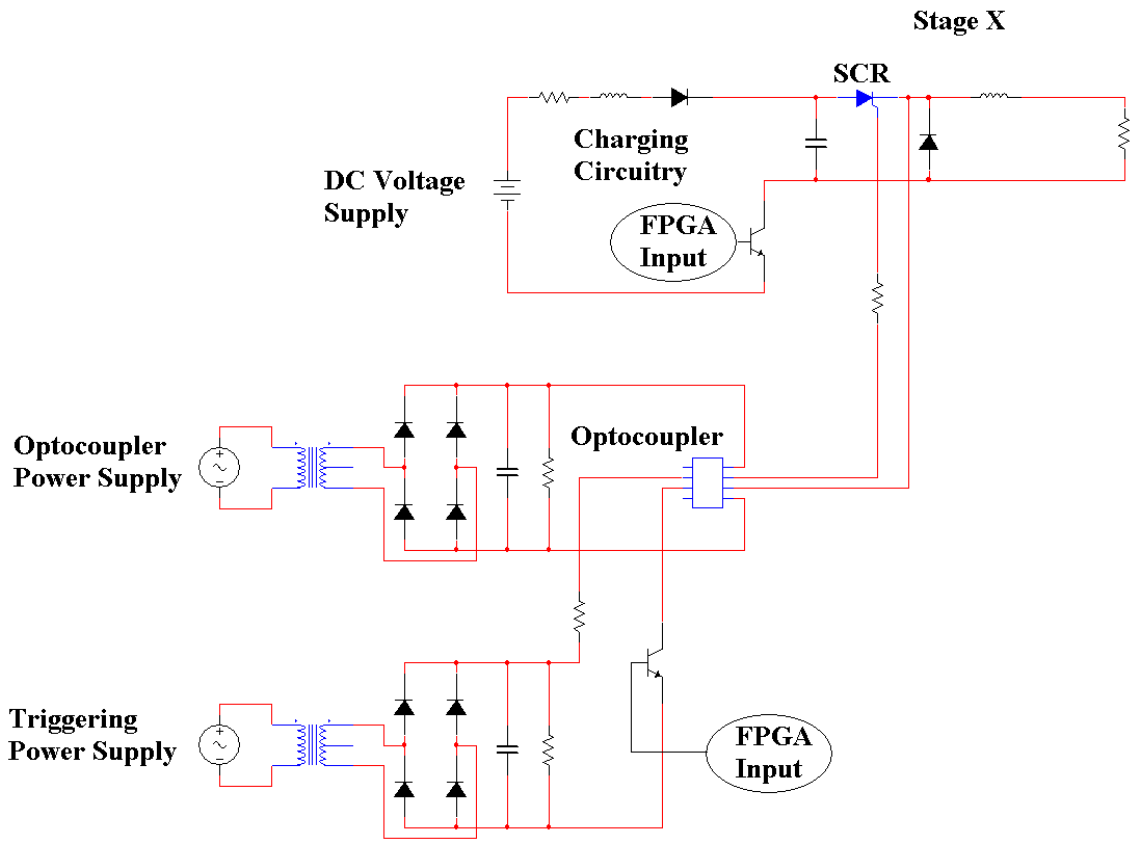

Figure 11: Complete Circuit for One Phase of the Pulse Forming Network

4.5 PFN FPGA Control

4.5.1 Controlling the inputs and outputs of the DE2 board

The pulse forming network was controlled using a state machine programmed into an Altera DE2 board. The block diagram of the program used is shown in the figure below.

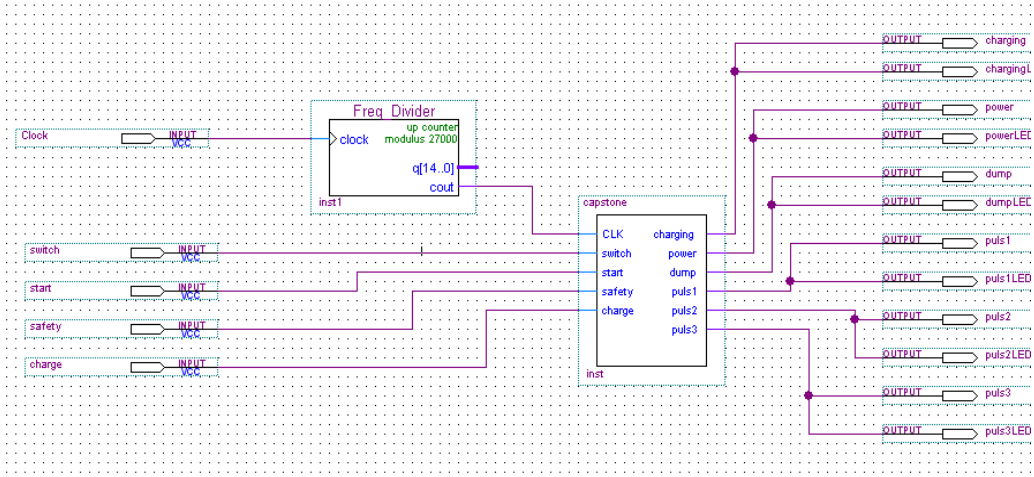

Figure 12: DE2 Board Control Program

The middle block in the figure is the state machine that controls the inputs and outputs of the DE2 board. There are five inputs and six outputs to the state machine. The inputs include a 27 MHz clock from the DE2 board, power input, charging trigger, safety switch, and pulse trigger. The 27 MHz clock is input to a frequency before entering the state machine to slow down the program's clock speed. The outputs are all wired to switches in the main circuit and provide gate signals that trigger power (puts the circuit in standby), capacitor charging, capacitor safety discharge, and firing of the capacitors to the simulated railgun load. The outputs are also tied to LEDs on the DE2 board for indication purposes. The VHDL code for the state machine is given in Appendix B.

A block diagram of the state machine is given in the figure below:

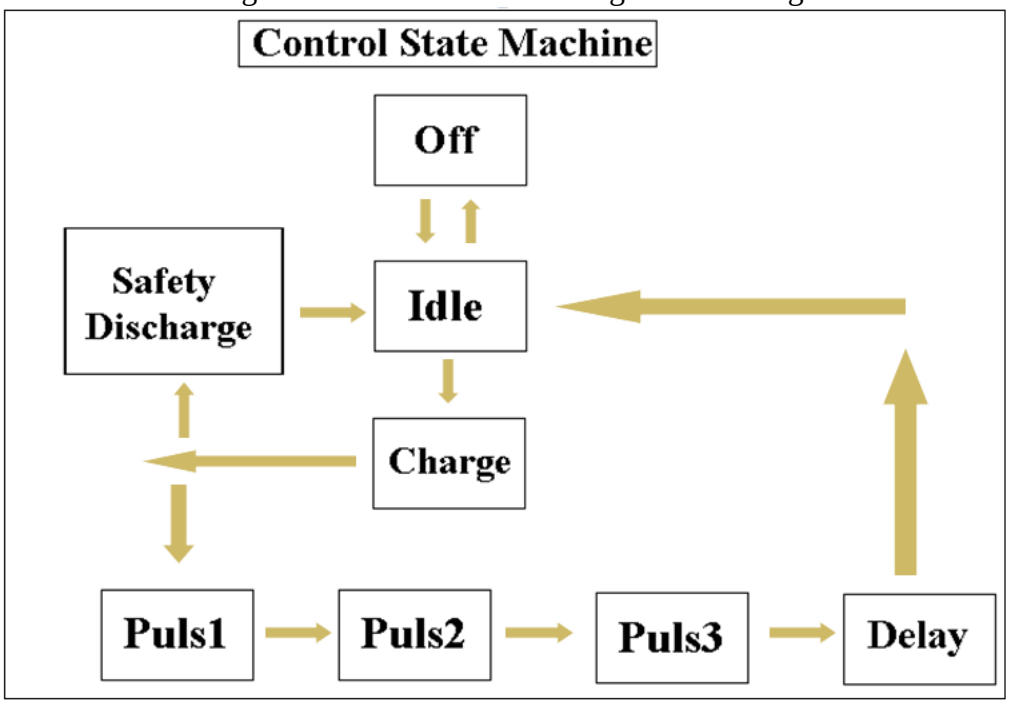

Figure 13: State Machine Diagram

The state machine's default state is the "Off" state. The program will always be in this state unless the power input is high. This state allows power to go to none of the components of the circuit, regardless of the other inputs. If the power input is made high into the DE2 board from the "Off" state, then the program goes into the "Idle" state. In this state power does not go to any of the elements of the circuit; however, the program is on standby waiting to either advance to the "Charge" state or back to the "Off" state. If the charge input into the DE2 board goes high then the program advances into the charge state. This state allows the capacitors to charge. At this time the state machine either advances to the "Safety Discharge" state or "Puls1" state depending on whether the safety input or pulse trigger input is made high. The "Safety Discharge" state triggers a switch that creates a path for the charge in the Capacitors to safely dissipate. The program then returns to the "Idle" state. The "Puls1" state begins the firing of the PFN. This state sends high signals to the first two capacitors firing circuits, causing them to discharge. The program then automatically advances to "Puls2" which fires the third capacitor, still holding high signals for the first two capacitors. "Puls2" automatically advances to

“Puls3” which discharges the last capacitor, maintaining the high outputs for the first three capacitor firing circuits. The program then advances to the “Delay” state and stays there until the pulse triggering input is made low again. This keeps the capacitor discharge signals high long enough for the capacitors to start discharging. A summary of the state outputs is given in Table 3 below:

	State						
Output		Power	Charging	Safety Discharge	Pulse 1	Pulse 2	Pulse 3
	Off	Low	Low	Low	Low	Low	Low
	Idle	High	Low	Low	Low	Low	Low
	Charge	High	High	Low	Low	Low	Low
	Safety Discharge	High	High	High	Low	Low	Low
	Puls1	High	High	Low	High	Low	Low
	Puls2	High	High	Low	High	High	Low
	Puls3	High	High	Low	High	High	High
	Delay	High	High	Low	High	High	High

Table 3: State Machine Inputs and Outputs

4.5.2 Controlling the Timing of the Pulses

All timing in the state machine was controlled by the clock of the state machine. The 27 MHz clock of the DE2 board was put through the frequency divider seen in Figure 12 so that the state machine operated on a one millisecond clock. Since one millisecond was the desired time between pulses, the pulse state merely had to sequentially run to achieve the correct timing.

To achieve a one millisecond pulse, the frequency divider counts the 27 MHz clock’s iterations 2^14 times and then produces a carry out. This carry out alternates every millisecond as the clock counts to the desired number again.

5 RESULTS

5.1 Simulation and Testing at 30 Volts

The pulse forming network was simulated and tested with 30 volts applied to the capacitors. The results were measured with a Rogowski coil. The results are illustrated in Figure 14. The peak current for the simulation was 145A. The peak current for the actual pulse forming network was 175A. The pulse width for the simulation and measured current was about 3ms.

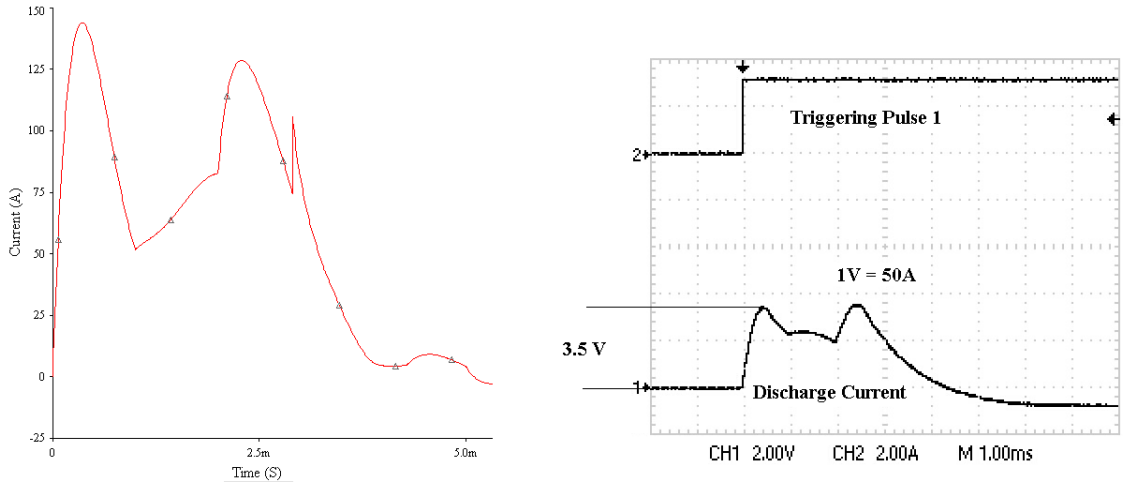

Figure 14: Results at 30 Volts

5.2 Simulation and Testing at 50 Volts

The pulse forming network was then simulated and tested with 50 volts applied to the capacitors. The results were again measured with a Rogowski coil. The results are illustrated in Figure 15. The peak current for the simulation was 245A. The peak current for the actual pulse forming network was 300A.The pulse width for the simulation and measured current was about 3ms.

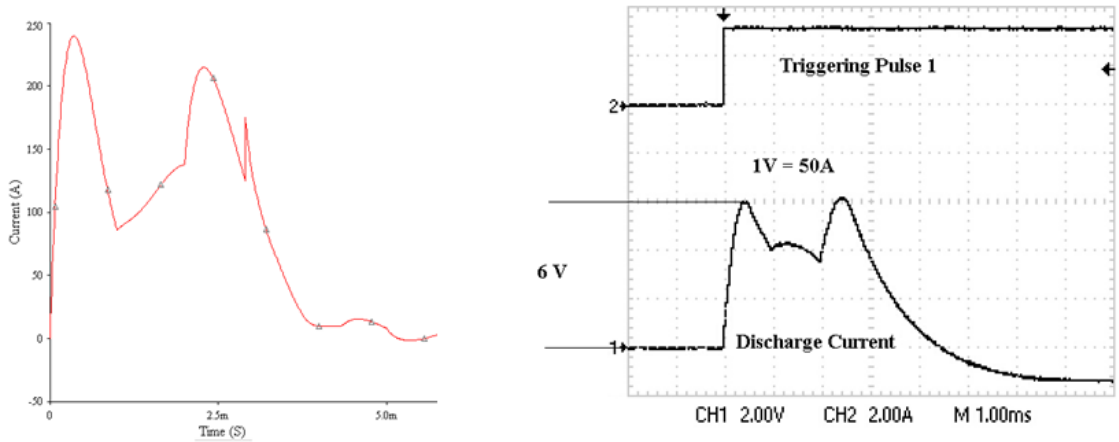

Figure 15: Results at 50 Volts

5.3 Simulation and Testing at 200 Volts

The pulse forming network was then tested with 200 volts applied to the capacitors. The results were not measured with a Rogowski coil because the device has a limit of 300A. Through extrapolation of our data, it was predicted that at 200V, there would be approximately 1200A of peak current in the pulse.

5.4 Simulation at 400 Volts

The pulse forming network was only simulated at 400 volts, because the SCR in the actual circuit was only rated to 1400 amps of pulsed current. It was extrapolated that at 400 volts, the load would receive a 2000 amp current pulse. Using multisim, that prediction was verified. The output current was calculated to be over 1900 amps. The waveform from Multisim is shown below in Figure 16.

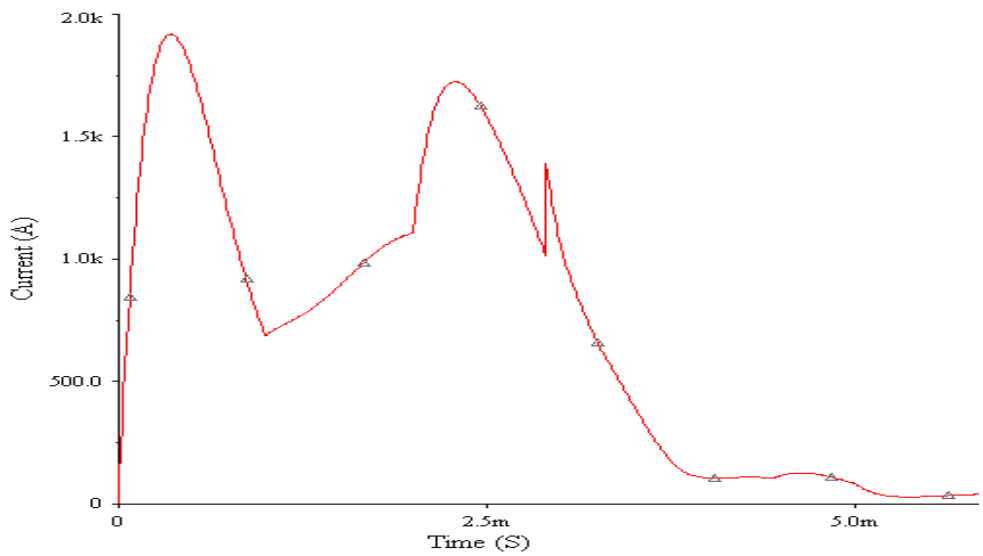

Figure 16: Simulated results at 400 Volts

6 CONCLUSIONS

6.1 Charging Circuit

Our charging time was somewhat lengthy at nearly 90 seconds. However, the resistance can be manipulated to change capacitor charging time. To increase charging time, lower input current, and create a safer charging cycle the resistance must be increased. To hasten the charging cycle, increase input current, and put more strain on the source and the individual components the resistance must be decreased.

6.2 Discharge Circuit

Overall the project met the specifications for the design and mirrored the results obtained through simulation. The shape and magnitude of the pulse was very similar to that of the simulation.

An interesting result was the effect of the load resistance of the magnitude of the current pulse. In the simulated waveform, the magnitude was slightly lower than the magnitude of the realized waveform from the project. It was determined that the cause of this disparity was due to an artificially high estimated load resistance. The load used for the pulse forming network was a simple high current-rated wire. The estimated load resistance used in the simulation was 100 mOhms, which was too high of an estimate and resulted in a lower than expected current magnitude.

6.3 Switching Circuit

The most significant problem encountered in achieving a successful test firing of the switching circuit was due to pulse time duration. Originally, the design was to create one millisecond pulses that were spaced one millisecond apart. However, through some debugging of the circuit and software it was determined that the one millisecond pulse proved to be to brief. By changing the gating pulses to turn on and stay on until instructed to turn off, the capacitors were able to be completely discharged and created the desired current pulse across the load.

7 IMPROVEMENTS FOR THE FUTURE

While the project was successful, there is much room for improvement and expansion of the project. The first improvement would be to design and assemble printed circuit boards for the charging, discharging, and switching circuits. Along with using printing circuit boards, the entire project could be made smaller and safer. To create a smoother current pulse, the inductors on the output of the capacitors would need to be manipulated, and more phases could be added. Due to the SCR's that were used this iteration of the project was limited to a current pulse of only 1400 amps. In order to have a circuit that could handle a higher current pulse, "hockey puck" SCR's could be used because of their higher rating. Finally, to truly test the project it could be paired with the actual railgun barrel and fired.

8 LESSONS LEARNED

The most important lessons learned from the completion of this project were not tangible. Rather, they were strategies that could be used for any project in the future. First, know exactly what needs to be done, create a basic design, and simulate it. If the results are reasonable and match what is expected, then build a small, low power version of the project. Each individual section of the project should be tested and verified. Once all of the sections work separately build a full-scale iteration of the project and integrate those sections gradually until the overall project works.

Appendix A: Safety Proposal

DIVISION OF ENGINEERING AND WEAPONS INSTRUCTION 5100
To: Chair Electrical and Computer Engineering Department
From: MIDN 1/C BALUCH, MIDN 1/C GARFRERICK, MIDN 1/C SCHIAVO
Via: Professor Ciezki and Prof. Firebaugh
Subj: RISK MANAGEMENT PROCEDURES FOR RAILGUN ULSE FORMING NETWORK CAPSTONE PROJECT

Ref: (a) USNA Instruction 5100.11C, Navy Occupational Safety and Health (NAVOSH)
Program Manual
(b) NSTM 300, Electrical Safety Manuel
(c) NASA NPG 8000.4 Risk Management Procedures and Guidelines

Encl: (1) Safety Plan Format

1. Purpose. This instruction establishes risk management guidelines and procedures for the railgun pulse forming network capstone project.

2. Background. This project will focus on the design and construction of the pulse forming network for the pre-built railgun. The pulse forming network will be simulated, constructed with hardware, and ultimately coupled to the railgun to test firing capability. All of these steps will be performed on the Naval Academy grounds. Because all testing will be done at USNA, recognizing situations that have the potential to cause people harm or to damage equipment and facilities, and taking appropriate measures to mitigate or eliminate the associated risks is important and is discussed in Enclosure 1.

Enclosure 1:
Hazard Identification

1) Accidental Discharge of Capacitors

Severity – I (Catastrophic)
Likelihood – E (Remote)

Description of Potential Hazard:
In the event that the capacitors were left in charged state at high voltage, the potential exist that someone could accidentally be electrocuted by the capacitor discharge.

Risk Mitigation:
1) The system will be enclosed in a protective covering.
2) The capacitors will always be left in the discharged state.
3) All charge/discharge sequences will be scheduled with the advisors.
4) LED lights that give a visual indication of the charged state will be operational
5) Charged capacitors will be discharged through the load bank or using the discharge circuit.
6) When the protective covering is removed, each capacitor will be manually discharged using either a grounding rod or the load bank, which will always be kept in the testing area.
7) After manual discharge, the voltage of each capacitor will be verified using a handheld digital multimeter.
8) Capacitors will only be charged to High Voltage with the intention to discharge the capacitor bank into the load bank or discharge the capacitors through the designed discharge circuit.

2) High Voltage Power Supply

Severity – I (Catastrophic)
Likelihood – E (Remote)

Description of Potential Hazard:
The high voltage power supply is capable of 450 V. This could electrocute a person who came in contact with exposed leads while at high voltage.

Risk Mitigation:
1) During testing all exposed connection to test equipment will be insulated.
2) In the final assembly all exposed connections will be internal to the protective case.
3) The power supply will be unplugged prior to opening the case.
4) The power supply will be unplugged when the unit is not in use.

3) Exploding Electronics/Fire

Severity – II (Severe Injury)
Likelihood – D (Improbable)

Description of Hazard:
The potential exists for the SCR (silicon controlled rectifiers) to come apart under a high current high voltage electrical pulse. The SCR's are rated to handle the anticipated current levels with a factor of safety. The capacitors can explode if they are reverse charged at high voltage.

Risk Mitigation:

1) All electronics and capacitors will be tested at low voltage when external to the protective case.
2) All high voltage tests will be conducted with the capacitors and electronics inside the protective case and inside an engine test cell.
3) The fire department will not need to be present for any testing.
4) The nearest fire extinguisher is in the Maury Hall power laboratory in which the group will do all testing. Along with the fire extinguisher, the power laboratory it outfitted with sprinklers.
5) The nearest fire alarm is in the hall way leading to the power laboratory

Appendix B: FPGA Code

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_misc.all;
use ieee.std_logic_unsigned.all;

entity capstone is

port (CLK,switch,start,safety, charge: in STD_LOGIC;
                charging,power,dump,puls1,puls2,puls3: out STD_LOGIC);

end capstone;

architecture run of capstone is

type STATE_TYPE is (OFF,DISCHARGE,CAP_CHARGE,IDLE,T1,T2,T3,delay);
        --defining all states
signal present_state, next_state : STATE_TYPE;
begin

        DEFAULT: process (CLK, switch)
        begin

                if(switch='0') then
                        present_state <= OFF;
                elsif (CLK'event and CLK='1') then
                        present_state <= next_state;
                end if;
        end process DEFAULT;

        ADVANCE: process(present_state,safety,start, switch, charge)

        begin
                case present_state is
                        when OFF =>
                                power <= '0';--signifies device off
                                dump  <= '0';--will not dump charge
                                charging <= '0';--capacitors will not be tied to source
                                puls1 <= '0';--capacitor release signals
                                puls2 <= '0';
                                puls3 <= '0';

                                if(switch = '1') then
```

```
                next_state <= IDLE;
        else
                next_state <= OFF;
        end if;

when IDLE =>
        power <= '1';
        dump  <= '0';--will not dump charge
        charging <= '0';--capacitors will not be tied to source
        puls1 <= '0';
        puls2 <= '0';
        puls3 <= '0';
        dump  <= '0';
        if(safety = '1') then
                next_state <= DISCHARGE;
        elsif (charge = '1') then
                next_state <= CAP_CHARGE;
        else
                next_state <= IDLE;
        end if;

        when CAP_CHARGE =>
        power <= '1';
        dump  <= '0';--will not dump charge
        charging <= '1';--capacitors will be tied to source
        puls1 <= '0';
        puls2 <= '0';
        puls3 <= '0';
        dump  <= '0';
        if(safety = '1') then
                next_state <= DISCHARGE;
        elsif (start = '1') then
                next_state <= T1;
        else
                next_state <= CAP_CHARGE;
        end if;

when DISCHARGE =>
        power <= '1';
        dump  <= '1';
        charging <= '0';
        puls1 <= '0';
        puls2 <= '0';
        puls3 <= '0';
        if(safety = '1') then
                next_state <= DISCHARGE;
```

```
                else
                        next_state <= IDLE;
                end if;


        when T1 =>
                power <= '1';
                puls1 <= '1';
                puls2 <= '0';
                puls3 <= '0';
                dump  <= '0';
                charging <= '0';
                next_state <= T2;

        when T2 =>
                power <= '1';
                puls1 <= '1';
                puls2 <= '1';
                puls3 <= '0';
                dump  <= '0';
                charging <= '0';
                next_state <= T3;

        when T3=>
                power <= '1';
                puls1 <= '1';
                puls2 <= '1';
                puls3 <= '1';
                dump  <= '0';
                charging <= '0';
                next_state <= delay;

        when delay=>
                power <= '1';
                puls1 <= '1';
                puls2 <= '1';
                puls3 <= '1';
                dump  <= '0';
                charging <= '0';
                if(start = '1') then
                        next_state <= delay;
                else
                        next_state <= IDLE;
                end if;

end case;
```

```
        end process ADVANCE;

end run;
```

References:

[1] "In, the Department of Defense Office of the Inspector General: . "USA 5"/62 (12.7 cm) Mark 45 Mod 4." *NavWeaps - Naval Weapons, Naval Technology and Naval Reunions - Navy Weapons*. N.p., n.d. Web. 8 Dec. 2010. <http://www.navweaps.com/Weapons/WNUS_5-62_mk45.htm>.