Asynchronous Serial Communications*

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Figure 1 shows asynchronous serial communications with a start bit and a single stop bit, along with N data bits. Successful communications require that the receiver sample the incoming data as well as the start and stop bits roughly in the center of each bit period. When the start bit is recognized, the receiver waits half a bit-period T_{bit} to establish time $t = 0$. It then samples the data stream at times $t \in \{T, 2T, 3T, \ldots, NT, (N+1)T\}$. However, there inevitably is some error in guessing these times—even in guessing the correct time to declare $t = 0$—since the clock driving the transmitter and the clock driving the receiver are not tightly synchronized but run completely independently of one another. Regarding the transmitter's clock as having zero error, $T_{\text{transmitter}} = T$ and we can ascribe all of the error to the receiver's clock. If we assume there could be up to time δt error in each half-bit period T then at time $t = nT_{\text{receiver}}$ the

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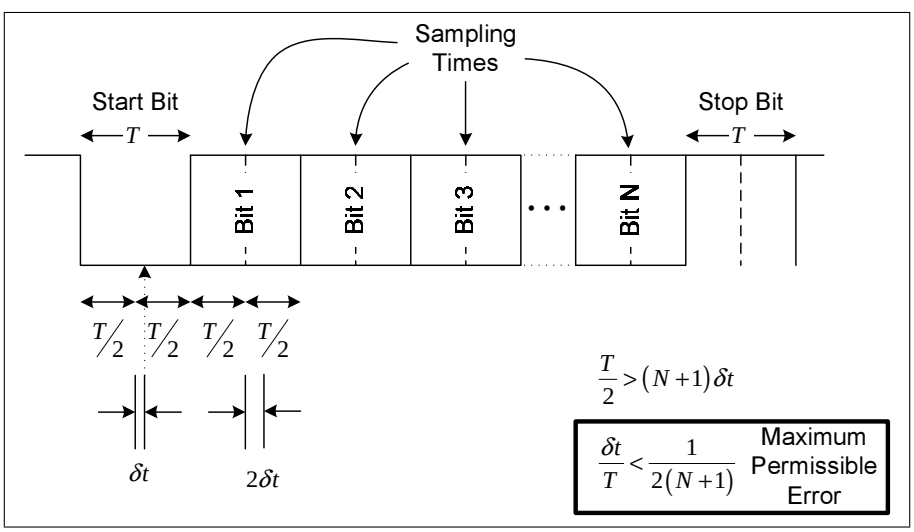

Figure 1: Maximum permissible error in asynchronous communications

transmitter's time will be

$$\begin{aligned} nT_{\text{receiver}} &= nT + (1 + 2(N+1))\delta t \\ &= nT + (2N+3)\delta t. \end{aligned}$$

Thus the cumulative error when the stop bit is sampled is $(2N+3)\delta t$. We require that this not exceed one half of the bit period T:

$$\begin{aligned} (2N+3)|\delta t| &< \frac{T}{2} \\ \frac{|2\delta t|}{T} &< \frac{1}{2N+3}. \end{aligned}$$

This expression represents the fractional permissible error in the receiver's clock during each nominal bit period T.

As an example, if the bit rate is 3000 bps then $T = 1/(3000\,\text{bps}) = 333\ \mu\text{s}$. If we transmit $N = 8$ data bits, then we require

$$\begin{aligned} |2\delta t| &< \frac{T}{2N+3} \\ &= \frac{333\ \mu\text{s}}{2(8)+3} \\ &= 17.5\ \mu\text{s}. \end{aligned}$$

In practice, this means that

$$\begin{aligned} T - |2\delta t| < T_{\text{receiver}} &< T + |22\delta t| \\ 333\ \mu\text{s} - 17.5\ \mu\text{s} < T_{\text{receiver}} &< 333\ \mu\text{s} + 17.5\ \mu\text{s} \\ 315.8\ \mu\text{s} < T_{\text{receiver}} &< 350.9\ \mu\text{s} \\ 2850\,\text{bps} > f_{\text{receiver}} &< 3167\,\text{bps}. \end{aligned}$$

This can also be expressed using relative error of the period or relative error of the bit rate:

$$\frac{T_{\text{receiver}} - T}{T} = \frac{|2\delta t|}{T} = 5.26\%$$

or

$$\frac{f_{\text{receiver}} - f}{f} = \frac{|2\delta f|}{f} \in [5.00\%, 5.56\%].$$

The error can be kept less than these extreme values with a PIC16F874—provided both the transmitter and the receiver are set to the same nominal bit rate.