EE461 Microprocessor-based Digital Design

Pulse Width Modulation

Solutions

1. For a PIC16F874 running with a 1.500 MHz crystal for its clock source, find settings for PR2, the TMR2 Prescale Value, and the 10-bit register `CCPR2L:CCP2CON(5 :4)` which will produce a duty cycle of 70% and a 1.010 kHz pulse width modulation frequency.

   It is not possible to achieve both of these values exactly. Choose parameters so that the desired pulse width modulation frequency is achieved as nearly as possible. Then choose remaining parameters so that the desired duty cycle is achieved as nearly as possible.

   What are the actual values of frequency and duty cycle which result? Express the error in both frequency and duty cycle as percentages.

   SOLUTION

$$T_{PWM} = 4(y + 1)T_{OSC}\,x$$

where

x = the Timer 2 prescaler value.

$X = \{1, 4, 16\}$,

and

y = PR2, the Timer 2 period register value y

$y = [0, 255]$.

So

$$x(y+1) = T_{pwm}/4T_{osc}$$

$$= \frac{1.500\text{ MHz}}{4\,(1.010\text{ kHz})}$$

$$= 371.3.$$

Only three values of the prescaler x are feasible. We can, therefore, choose a value y for the period register for each of these:

$$y = \frac{371}{x} - 1$$

and gather the values of y in a table. From these we can compute the values of T_{PWM}, $f_{PWM} = 1/T_{PWM}$, and the relative error

$$P_f = \frac{f_{achieved} - f_{desired}}{f_{desired}}.$$

The three choices for y and their effects are shown in this table:

x	y	T_{PWM}	f_{PWM}	P_f
1	370.3 ≈ 370	989.3 µs	1.011 kHz	0.07739%
4	91.82 ≈ 92	992.0 µs	1.008 kHz	—0.1916%
16	22.21 ≈ 22	981.3 µs	1.019 kHz	0.8932%

Naïvely we might suppose the pair $x = 1$ and $y = 370$ was best because it leads to the smallest relative error. However, y is only represented with eight bits, so $0 \le y \le 255$. The first row in the table violates this restriction. Therefore, the second row contains the best solution.

The duty cycle η can be found from

$$\eta = w / 4(y+1).$$

Solving this for w yields

$$\begin{aligned} w &= 4(y+1)\eta \\ &= 4(92 + 1)(0.70) \\ &= 260.4 \\ &\approx 260. \end{aligned}$$

Therefore, the actual duty cycle achieved is

$$\eta = 260 / 4(92 + 1) = 69.89\%$$

so the relative error in the duty cycle is

$$\begin{aligned} P_{?1} &= \frac{69.89\% - 70.0\%}{70.0\%} \\ &= -0.1536\%. \end{aligned}$$