EE461 Microprocessor-based Digital Design

Parallel Slave Port

Solutions

1. Suppose a PIC16F874 is operating under the control of an external processor using the PIC's Parallel Slave Port. The PIC has a clock crystal of frequency f_{OSC} = 18 MHz. What is the maximum possible delay before the external device's Write command is completed, that is, before the PIC16F874 successfully captures the data being supplied by the external device? What is the minimum possible delay? (To answer this question you will need to consider carefully the waveforms associated with the Parallel Slave Port. Assume that CS and WR both are asserted simultaneously and that the data are successfully captured when the IBF flag is set.)

SOLUTION

The PIC16F874 captures the incoming data from the external master at the start of the Q4 cycle which follows the next occurring Q2 cycle. The worst possible case—the longest possible delay—would occur if the master requested that the PIC accept data too late to meet this timing requirement. That is, if the master just missed a Q2 cycle then the PIC would not have another opportunity to capture the data until the next following Q2 cycle occurred, four machine cycles later. It then would have to wait one additional machine cycle for the start of the next Q4 cycle, at which point it would finally capture the data. Thus the maximum possible delay is five machine cycles.

Dmax = 5*Tosc = 5/fosc = 5/18Mhz = 278ns.

The minimum possible delay would occur if the master were to request that the PIC capture data just in time, that is, just at the end of a Q2 cycle. It would then only have to wait for one cycle, when the next Q4 cycle takes place. So the minimum possible delay is

Dmin = Tosc = 1/fosc = 1/18Mhz = 56ns.

2. If you decide to use the Parallel Slave Port, what is the maximum number *n* of analog input pins you can use? How many ways are there to specify the A/D Port Configuration Control bits so as to be able to specify that *n* analog input pins be used? Explain your answer.

SOLUTION

The Parallel Slave Port requires the use of bits 0, 1, and 2 in Port E for control by the external master. These bits could otherwise be used for analog inputs but the two uses are mutually exclusive. Therefore, instead of the maximum eight inputs, only five are available when the Parallel Slave Port is in use.

Several values of the bits PCFG3:PCFG0 = ADCON1(3:0) allow for the three bits in Port E to be used for supporting the Parallel Slave Port and for the remaining five possible analog inputs all to be dedicated to this purpose. These values are 0010 (five analog inputs); 0011 (four analog inputs and a positive voltage reference V_{+REF}; and 1100 (three analog inputs and both a positive voltage reference V_{+REF} and a negative voltage reference V_{-REF}.) Therefore, there is a total of three ways to have five analog input pins used while using the Parallel Slave Port.