EE461 Microprocessor-based Digital Design

Watchdog Timer

1. Your program's main loop in a PIC16F874 completes one iteration in no more than 250 ms. You decide to have it clear the watchdog timer at the start of every loop, even if the loop completes in less than this amount of time. What are the only permissible settings for the watchdog timer postscaler (that is, the Timer 0 prescaler?)

SOLUTION

Minimum, typical, and maximum times for the watchdog timer to time out is given in this table:

PS2:PS0	WDT Rate	Minimum /s	Typical /s	Maximum /s
000	1:1	0.007	0.018	0.033
001	1:2	0.014	0.036	0.066
010	1:4	0.028	0.072	0.132
011	1:8	0.056	0.144	0.264
100	1:16	0.112	0.288	0.528
101	1:32	0.224	0.576	1.056
110	1:64	0.448	1.152	2.112
111	1:128	0.896	2.304	4.224

To guarantee clearing of the watchdog timer before it times out, it cannot be permitted to operate in any setting that might cause it to time out in less than 250 ms. Only the last two rows meet this condition, so PS2:PS0 could be either 110 or 111.

2. Suppose the `T1CON` register contains the value 001001112. Discuss the effect this setting has on the ability of Timer 1 to bring the PIC16F874 out of the sleep state.

SOLUTION

If Timer 1 is operating as an asynchronous counter, then it can bring the processor out of the sleep state.

Because the `TMR1ON` bit (bit 0 of `T1CON`) is a 1, Timer 1 is enabled.

Because the `T1OSCEN` bit (bit 3 of `T1CON`) is 0, the oscillator is shut off. This is consistent with operation as a counter; if the oscillator were enabled, Timer 1 would operate as a timer, not a counter.

The `T1SYNC` (bit 2 of `T1CON`) is 1 and the `TMR1CS` bit (bit 1 of `T1CON`) is 1, so the external input on the `T1CKI` input can drive Timer 1 and no synchronization of this input is done. This is what makes Timer 1 operate in the asynchronous mode.

Therefore, Timer 1 can bring the PIC out of sleep state because it is operating, it is being driven by an external signal, and it is operating asynchronously.