Fast RAM (0400–06FF)

A_9	A_8	$\overline{CS_0}$	$\overline{CS_1}$
0	0	$A_{13} + A_{12}$	$A_9 + A_8$
0	1	$A_{13} + A_{12}$	$A_9 + \overline{A_8}$
1	0	$A_{13} + A_{12}$	$\overline{A_9} + A_8$

Fast RAM Chip Select Logic

ACIA (1000–1007)

A_2	A_1	CS_0	$\overline{CS_1}$	$\overline{CS_2}$
0	0	$\overline{A_{13}}\ A_{12}\ \overline{A_5}\ \overline{A_4}$	A_2	A_1
0	1	$\overline{A_{13}}\ A_{12}\ \overline{A_5}\ \overline{A_4}$	A_2	$\overline{A_1}$
1	0	$\overline{A_{13}}\ A_{12}\ \overline{A_5}\ \overline{A_4}$	$\overline{A_2}$	A_1
1	1	$\overline{A_{13}}\ A_{12}\ \overline{A_5}\ \overline{A_4}$	$\overline{A_2}$	$\overline{A_1}$

ACIA Chip Select Logic

PIA (1010–1013)

CS_0	$\overline{CS_1}$	$\overline{CS_2}$
A_{12}	A_{13}	$\overline{A_4}$

PIA Chip Select Logic

Buffer (1020–1022)

A_1	A_0	G_0	$\overline{G_1}$
0	0	$\overline{A_{13}}\ A_{12}\ A_5$	$A_1 + A_0$
0	1	$\overline{A_{13}}\ A_{12}\ A_5$	$A_1 + \overline{A_0}$
1	0	$\overline{A_{13}}\ A_{12}\ A_5$	$\overline{A_1} + A_0$

Buffer Chip Select Logic

ROM (2800–37FF)

OE_1	$\overline{OE_2}$
A_{13}	0

ROM Chip Select Logic