

Figure 1.1: Engineering Design.

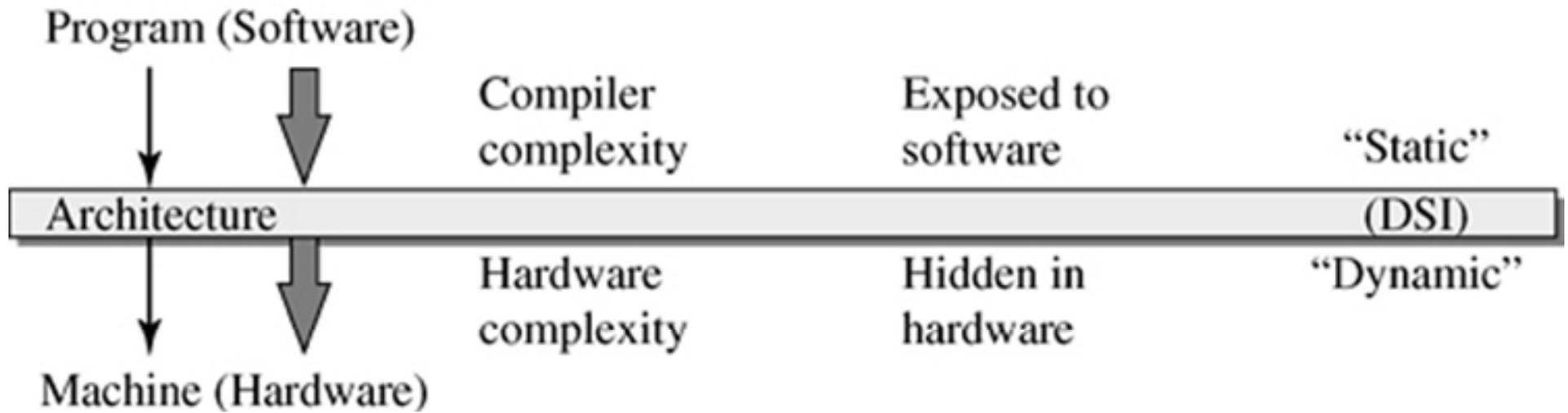


Figure 1.2 The Dynamic-Static Interface.

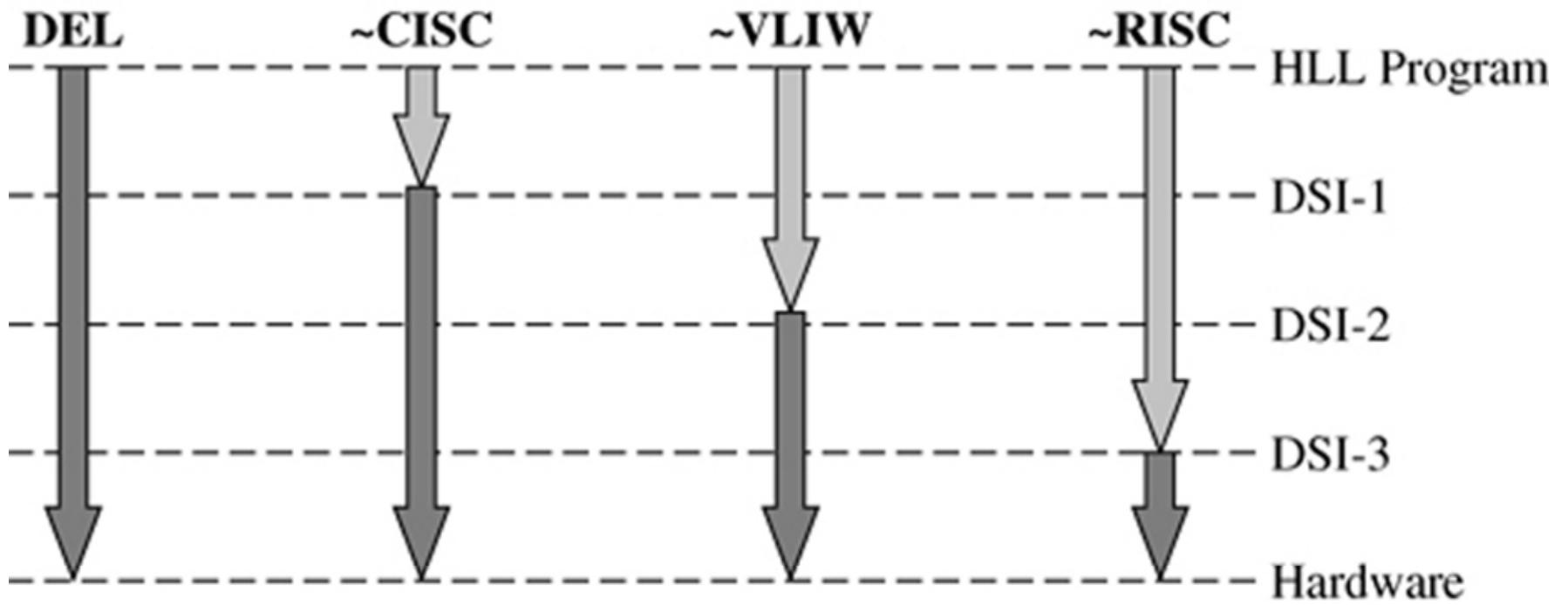
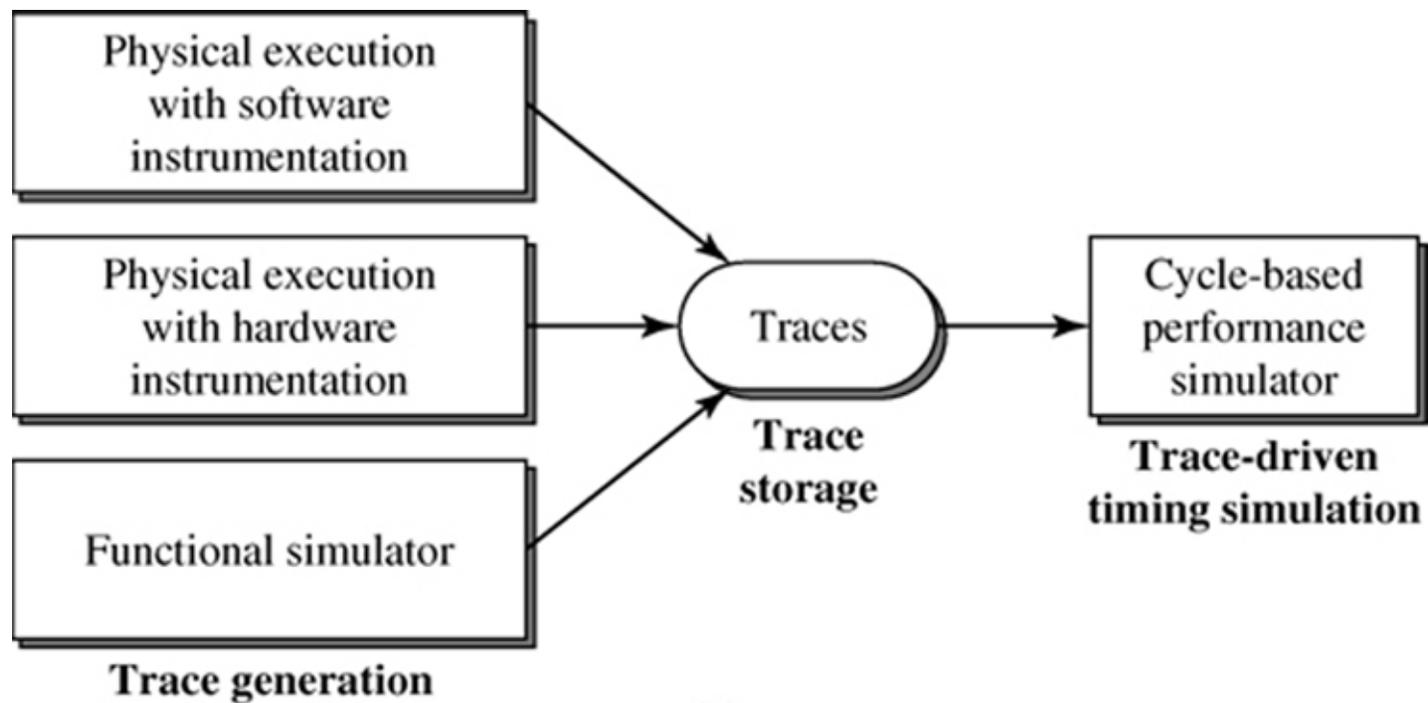
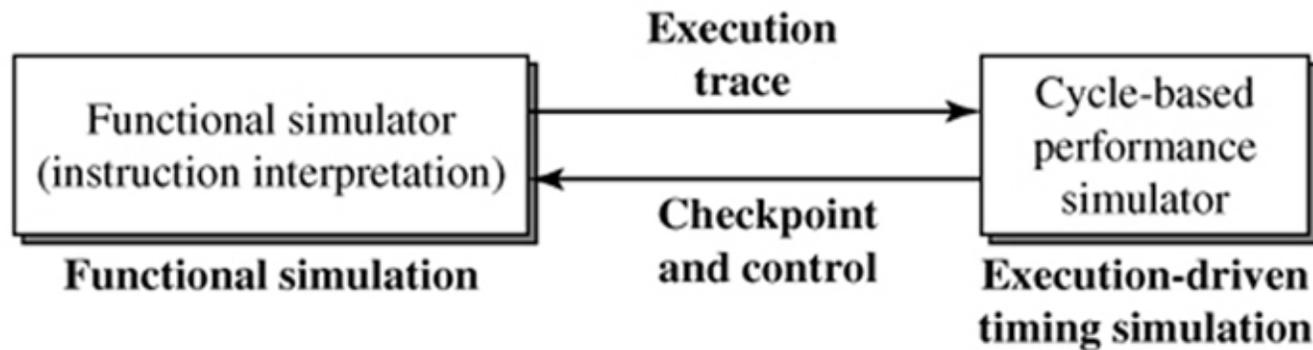


Figure 1.3: Conceptual Illustration of Possible Placements of DSI in ISA Design.



(a)



(b)

Figure 1.4: Performance Simulation Methods: (a) Trace-Driven Simulation; (b) Execution-Driven Simulation.

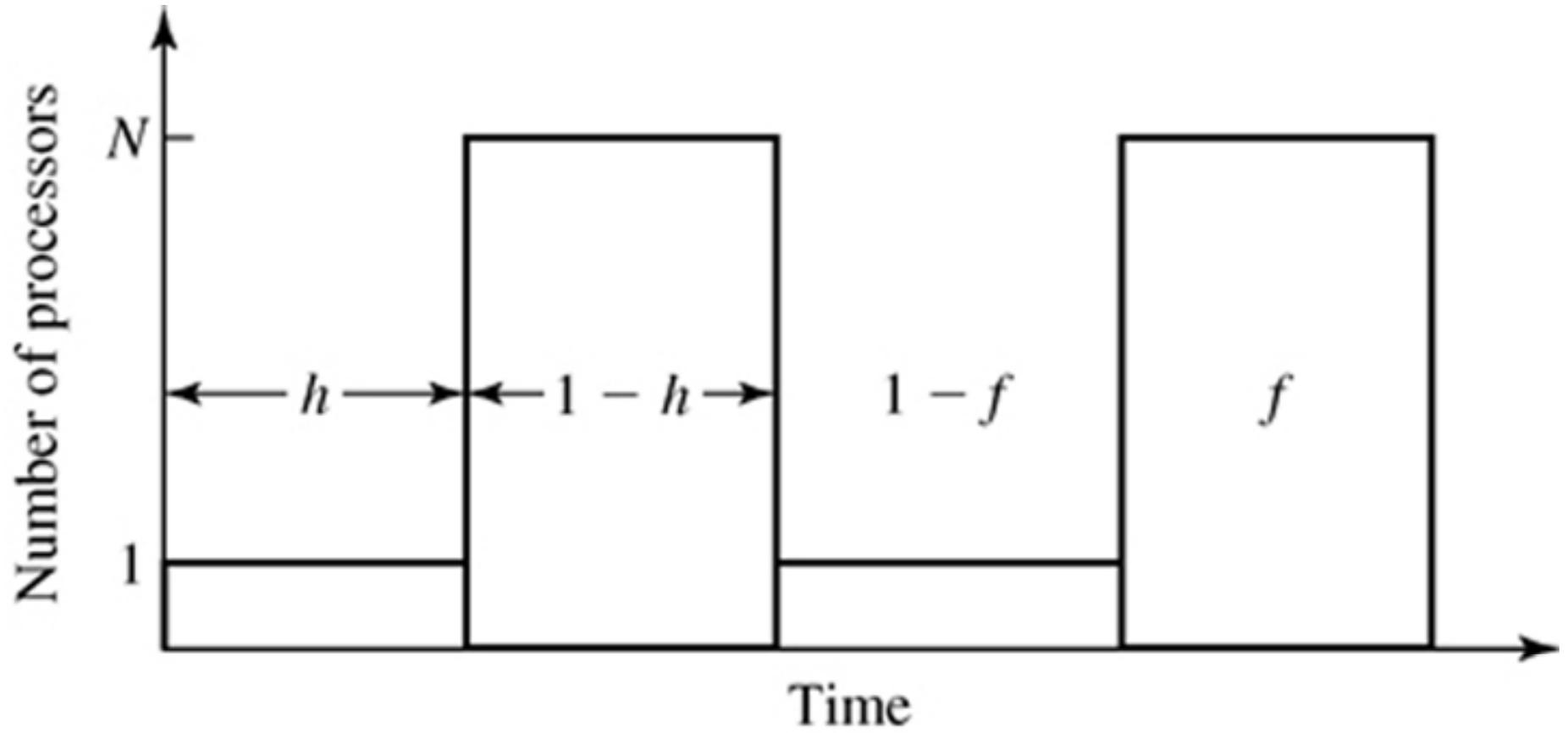
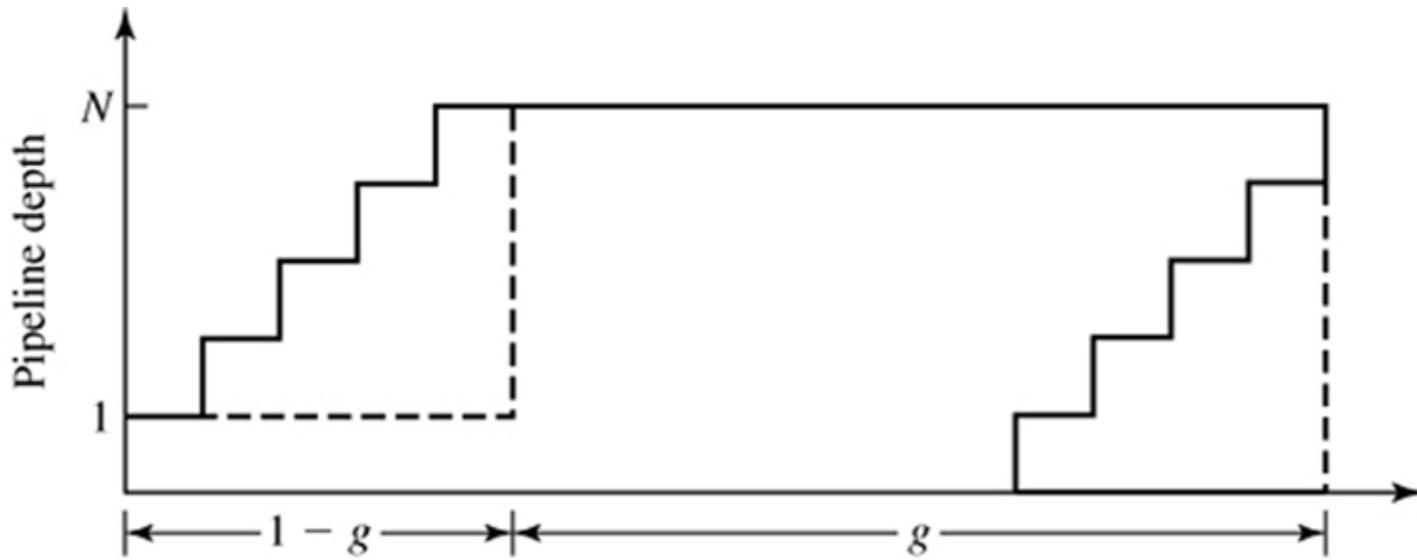
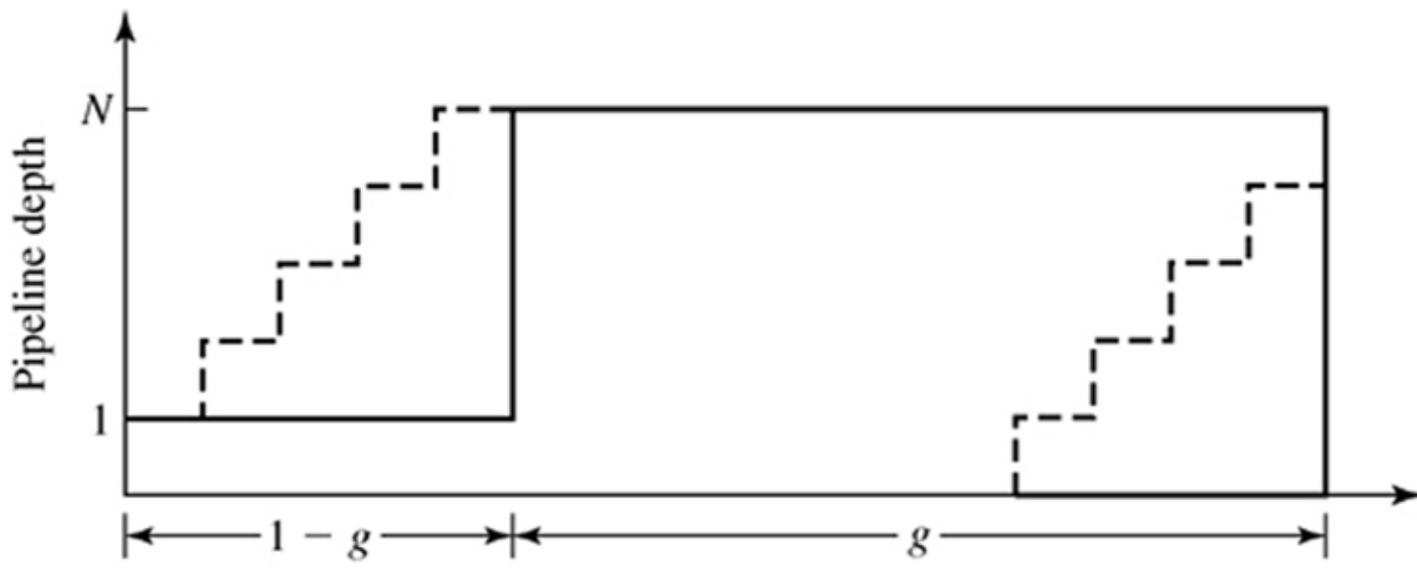


Figure 1.5: Scalar and Vector Processing in a Traditional Supercomputer.

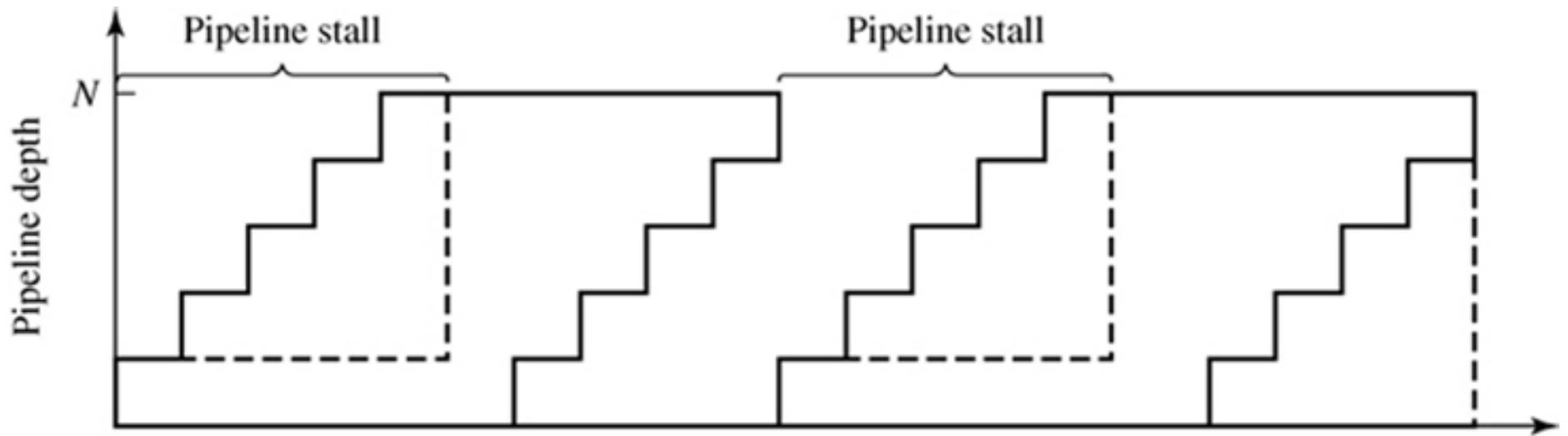


(a)

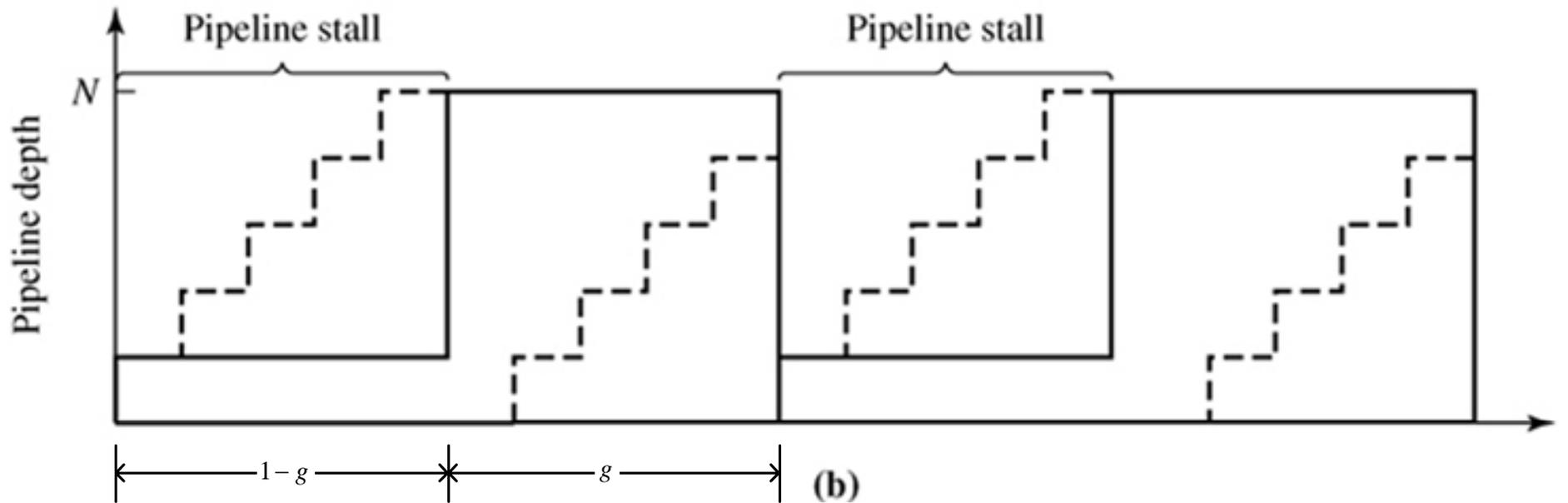


(b)

Figure 1.6: Idealized Pipelined Execution Profile: (a) Actual; (b) Modeled.



(a)



(b)

Figure 1.7: Realistic Pipeline Execution Profile: (a) Actual; (b) Modeled

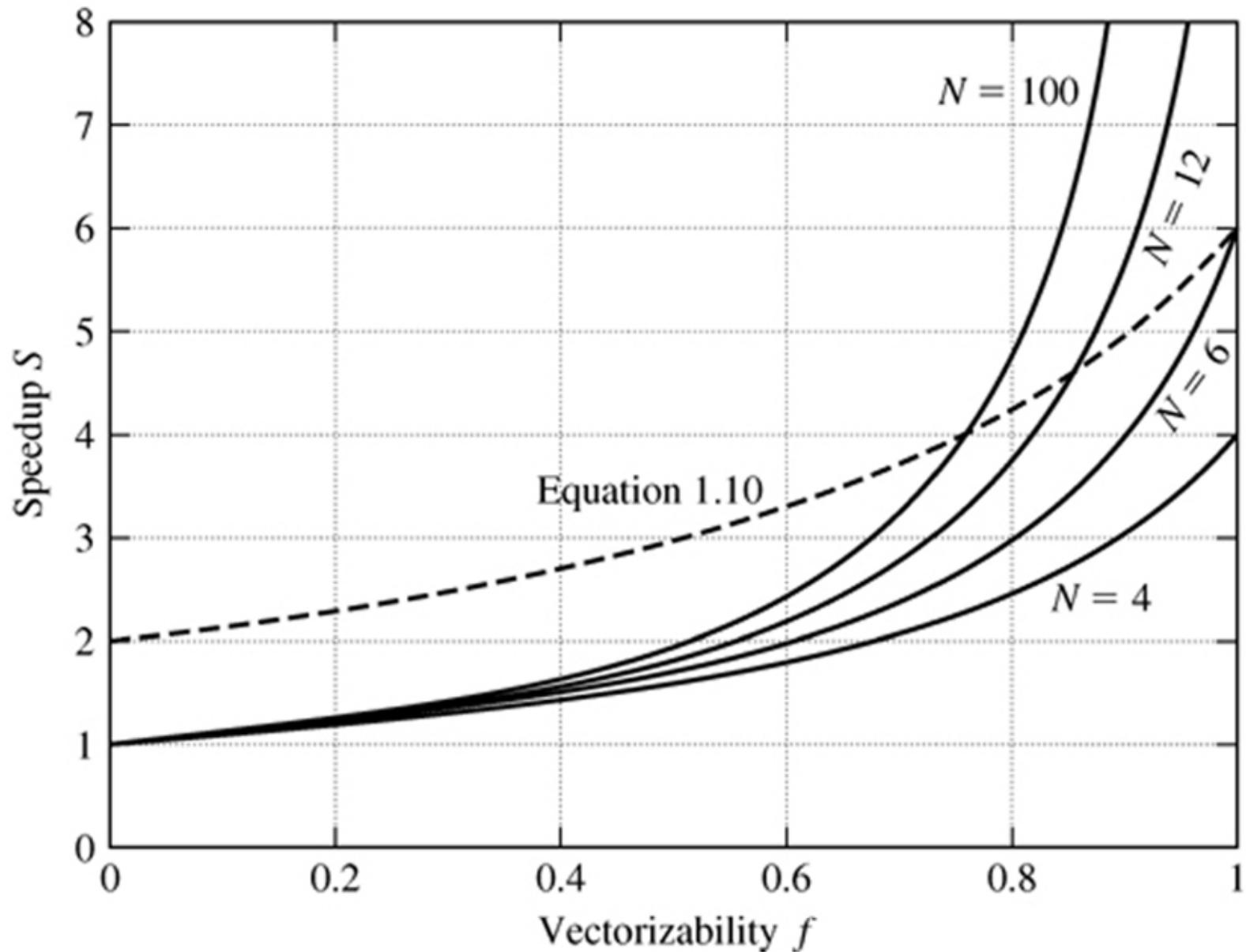


Figure 1.8: Easing of the Sequential Bottleneck with Instruction-Level Parallelism for Nonvectorizable Code.

Source: Agerwala and Cocke, 1987.

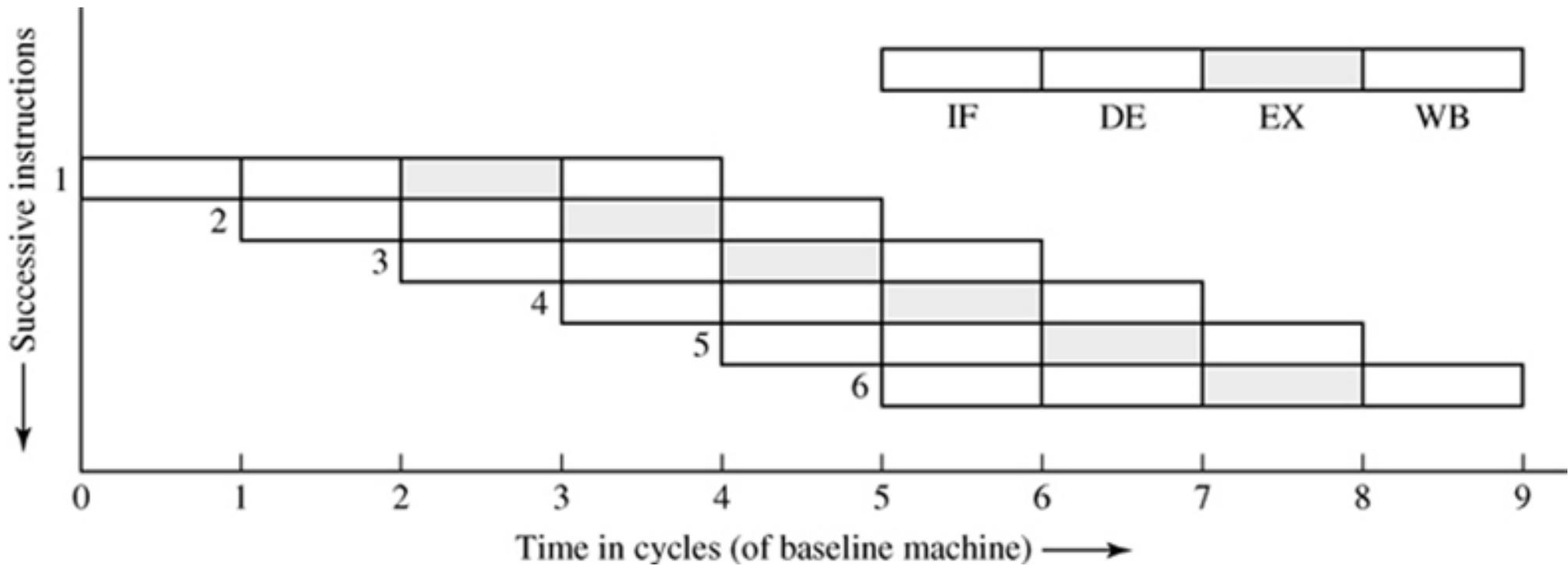


Figure 1.9: Instruction Processing Profile of the Baseline Scalar Pipelined Machine.

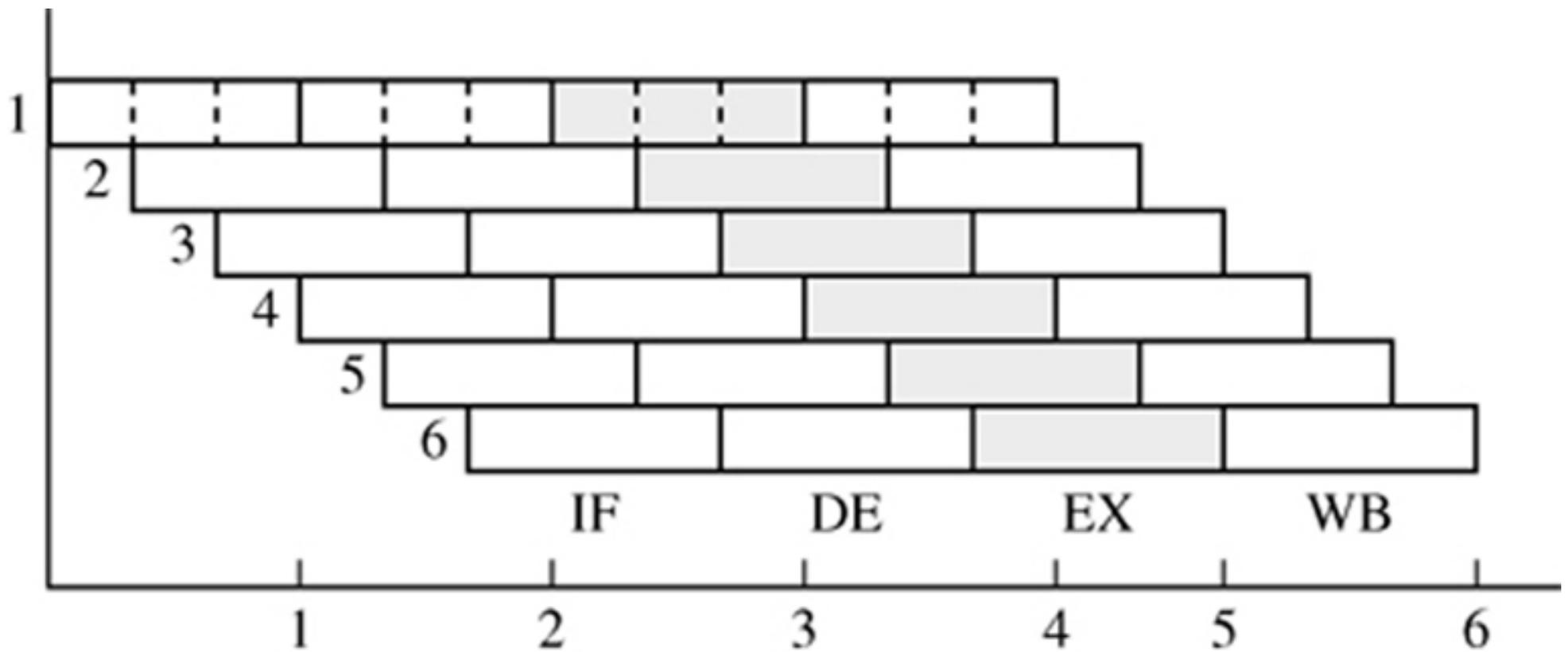


Figure 1.10: Instruction Processing Profile of a Superpipelined Machine of Degree $m=3$.

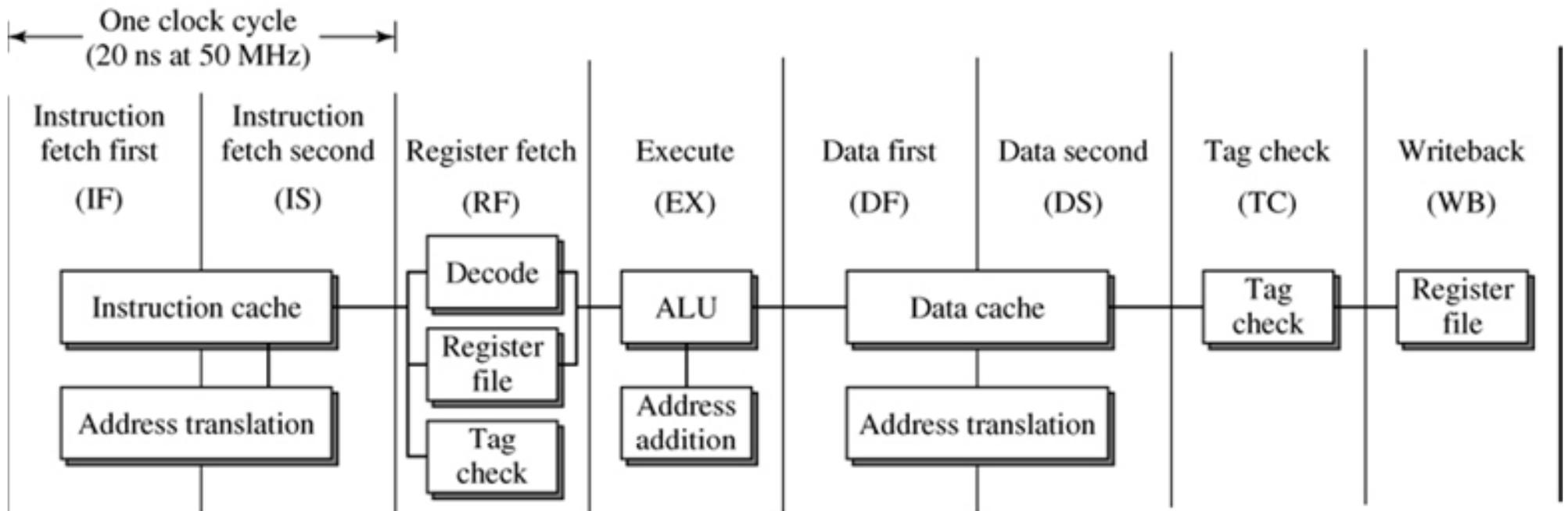


Figure 1.11: The “Superpipelined” MIPS R4000 8-Stage Pipeline.

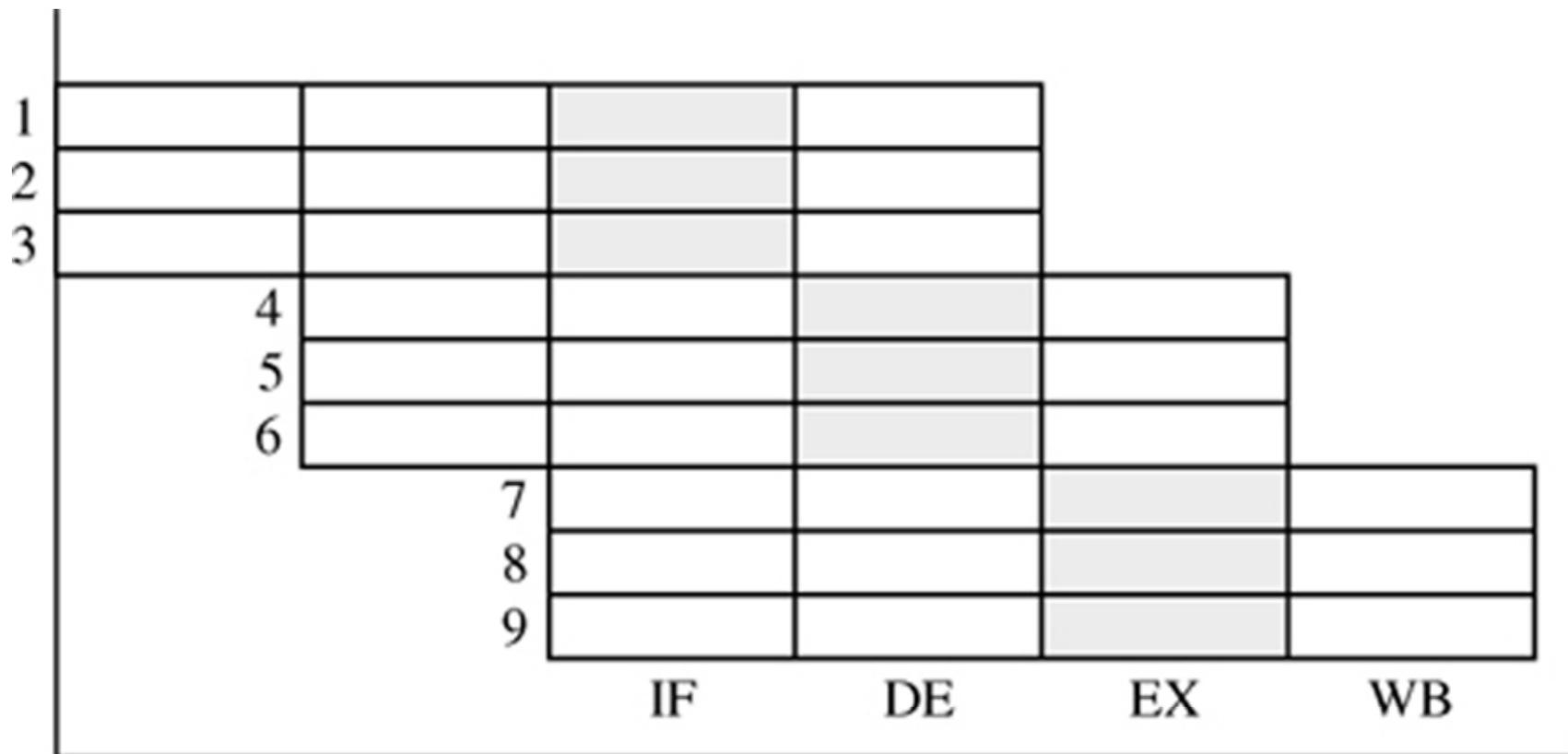


Figure 1.12: Instruction Processing Profile of a Superscalar Machine of Degree $n=3$.

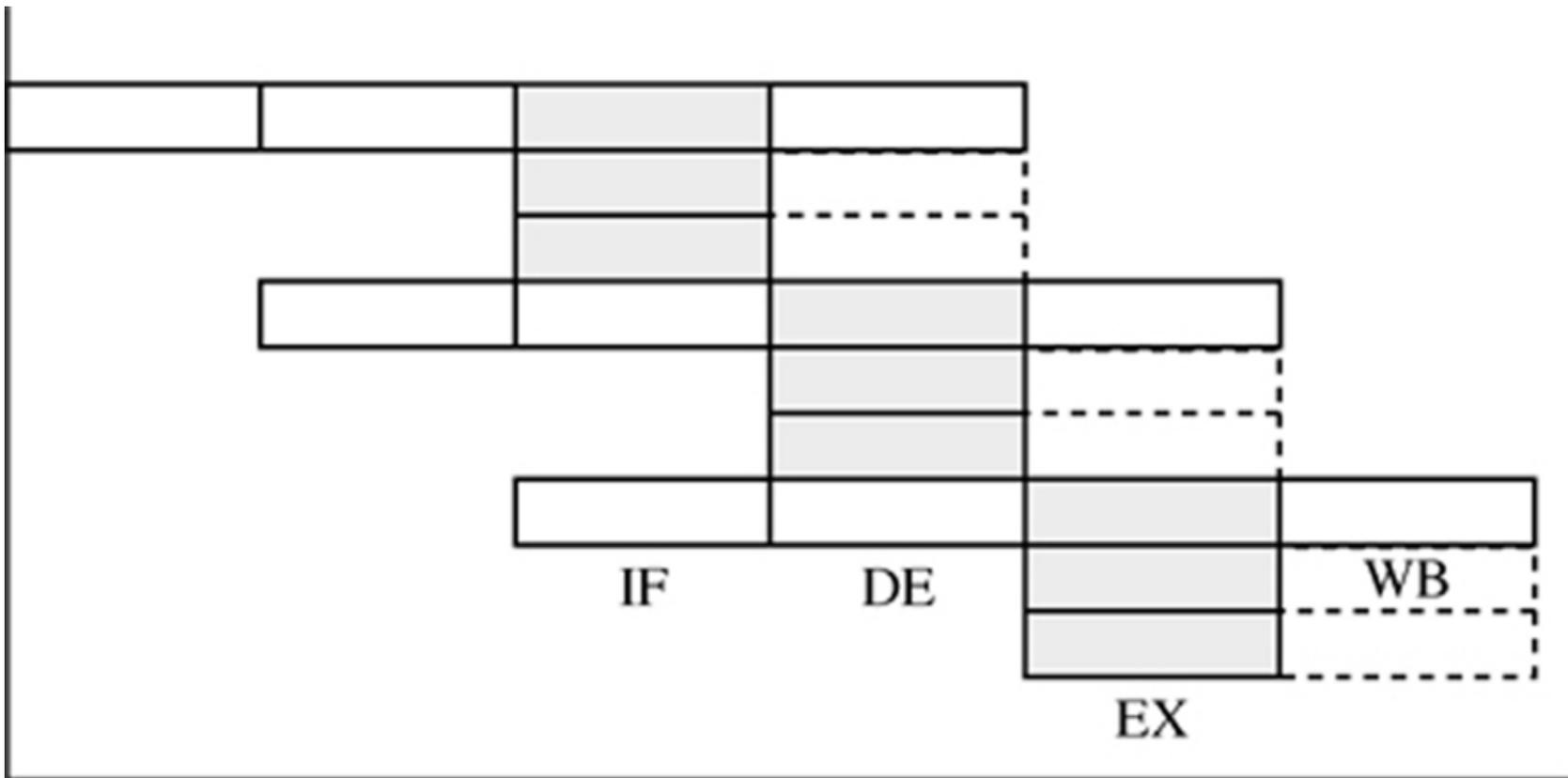


Figure 1.13: Instruction Processing Profile of a VLIW Machine of Degree $n=3$.