

Table 2.6

Worst-case penalties due to RAW hazards in the TYP pipeline when forwarding paths are used

	Leading Instruction Type (<i>i</i>)		
	ALU	Load	Branch
Trailing instruction types (<i>j</i>)	ALU, Load/Store, Br.	ALU, Load/Store, Br.	ALU, Load/Store, Br.
Hazard register	Int. register (R _i)	Int. register (R _i)	PC
Register write stage (<i>i</i>)	WB (stage 6)	WB (stage 6)	MEM (stage 5)
Register read stage (<i>j</i>)	RD (stage 3)	RD (stage 3)	IF (stage 1)
Forward from outputs of:	ALU, MEM, WB	MEM, WB	MEM
Forward to input of:	ALU	ALU	IF
Penalty w/ forwarding paths	0 cycles	1 cycle	4 cycles

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