Table 2.7
Functionality of the MIPS R2000/R3000 five-stage pipeline

Stage Name	Phase	Function Performed
1. IF	$\phi 1$	Translate virtual instruction address using TLB.
	$\phi 2$	Access I-cache using physical address.
2. RD	$\phi 1$	Return instructions from I-cache; check tags and parity.
	$\phi 2$	Read register file; if a branch, generate target address.
3. ALU	$\phi 1$	Start ALU operation; if a branch, check branch condition.
	$\phi 2$	Finish ALU operation; if a load/store, translate virtual address.
4. MEM	$\phi 1$	Access D-cache.
	$\phi 2$	Return data from D-cache; check tags and parity.
5. WB	$\phi 1$	Write register file.
	$\phi 2$	—

Table 2.7: Functionality of the MIPS R2000/R3000 five-stage pipeline.