Table 2.8
Functionality of the Intel 486 five-stage pipeline

Stage Name	Function Performed
1. Instruction fetch	Fetch instruction from the 32-byte prefetch queue (prefetch unit fills and flushes prefetch queue).
2. Instruction decode-1	Translate instruction into control signals or microcode address. Initiate address generation and memory access.
3. Instruction decode-2	Access microcode memory. Output microinstruction to execute unit.
4. Execute	Execute ALU and memory accessing operations.
5. Register write-back	Write back result to register.

Table 2.8: Functionality of the Intel 486 five-stage pipeline.