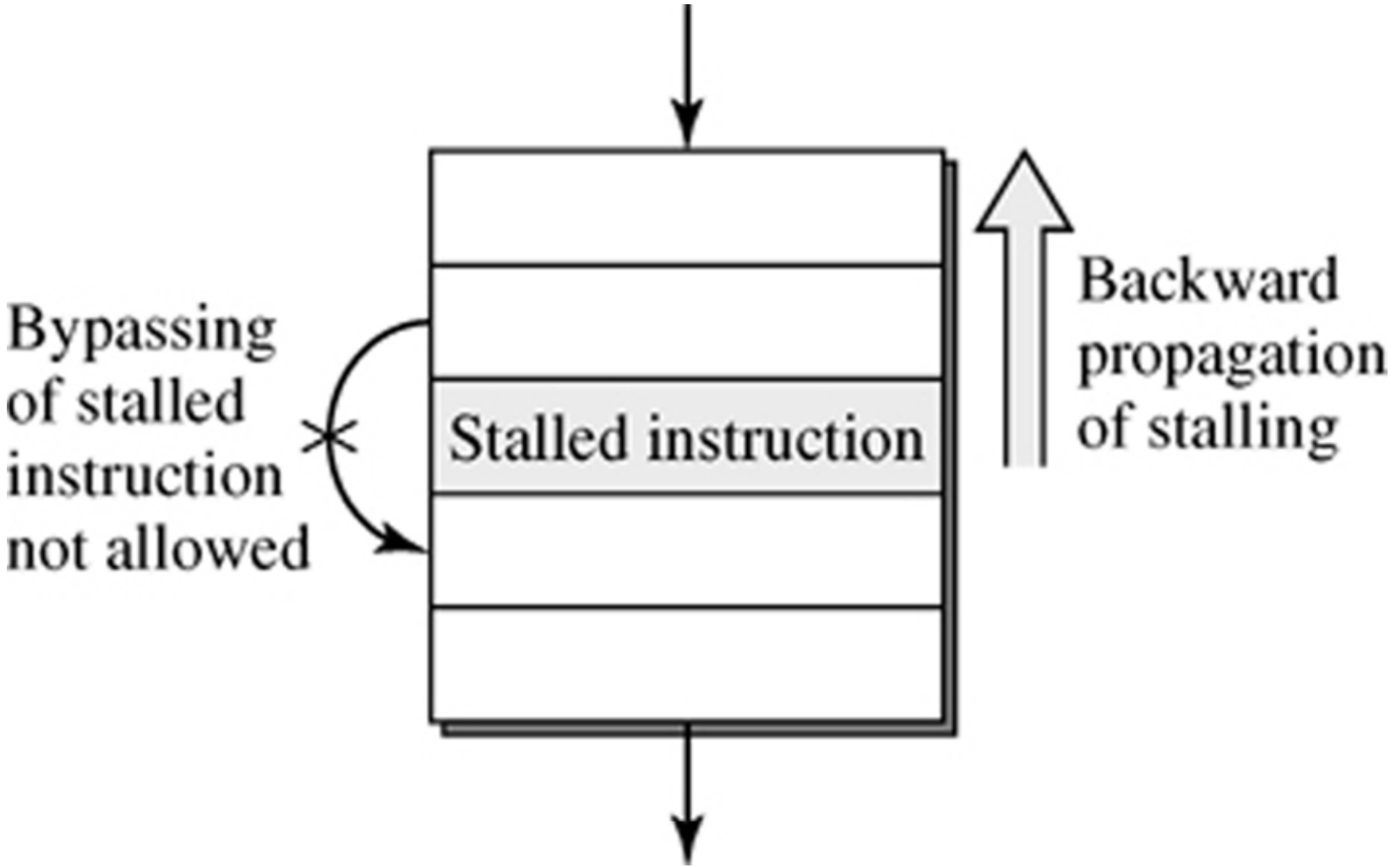

Figure 4.1: Unnecessary Stall Cycles Induced by Backward Propagation of Stalling in a Rigid Pipeline.

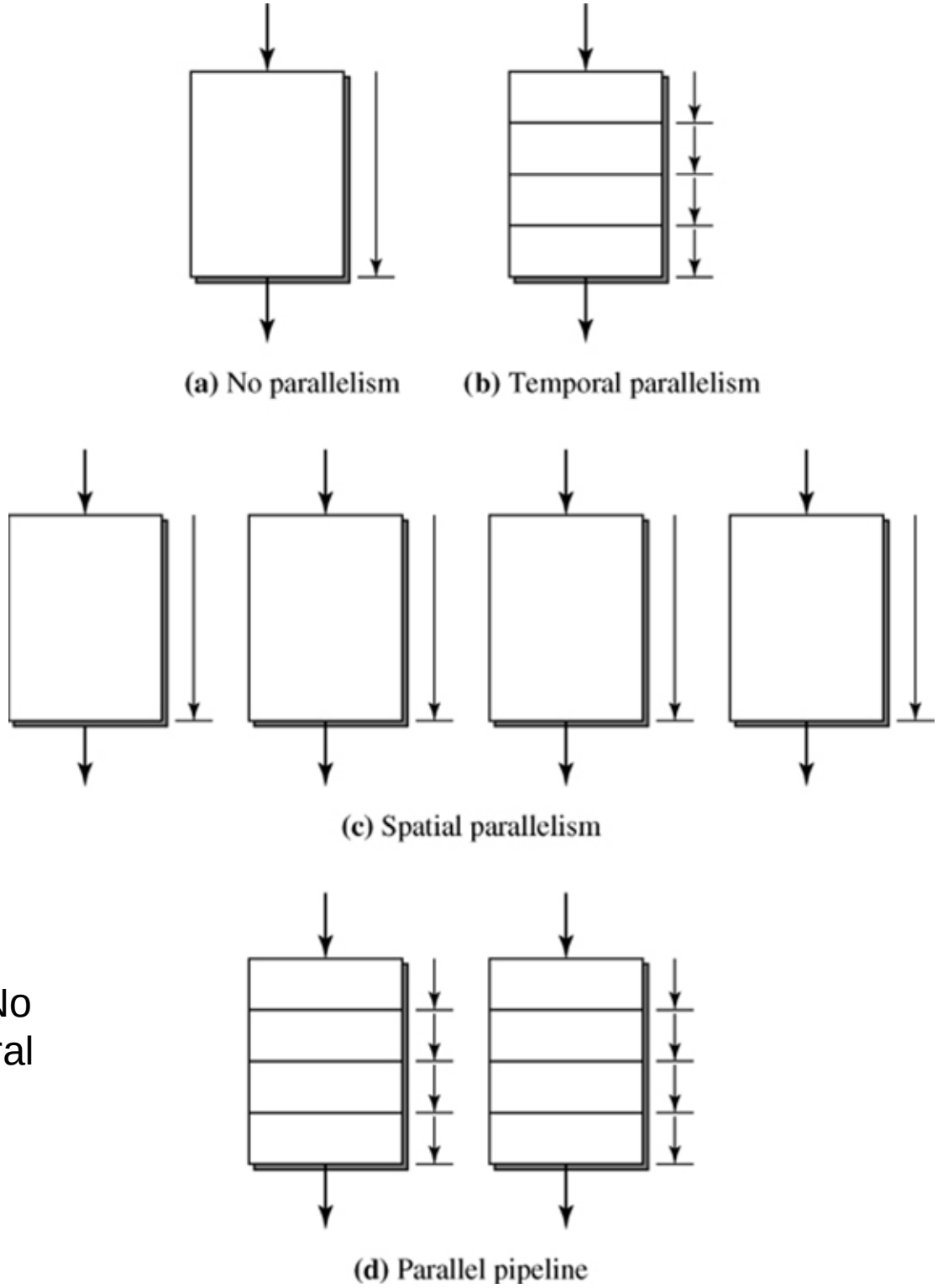

Figure 4.2: Machine Parallelism: (a) No Parallelism (Nonpipelined); (b) Temporal Parallelism (Pipelined); (c) Spatial Parallelism (Multiple Units); (d) Combined Temporal and Spatial Parallelism.

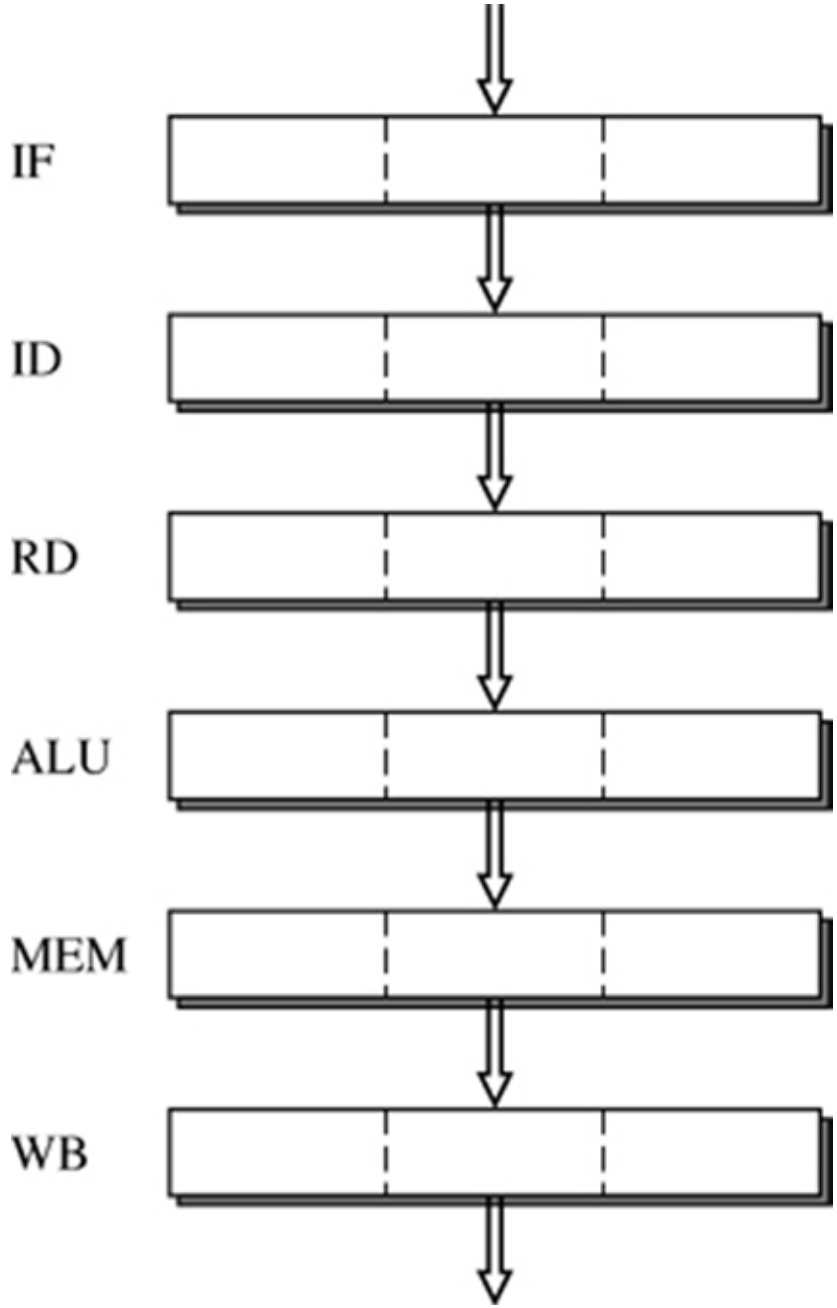

Figure 4.3: A Parallel Pipeline of Width *s*=3.

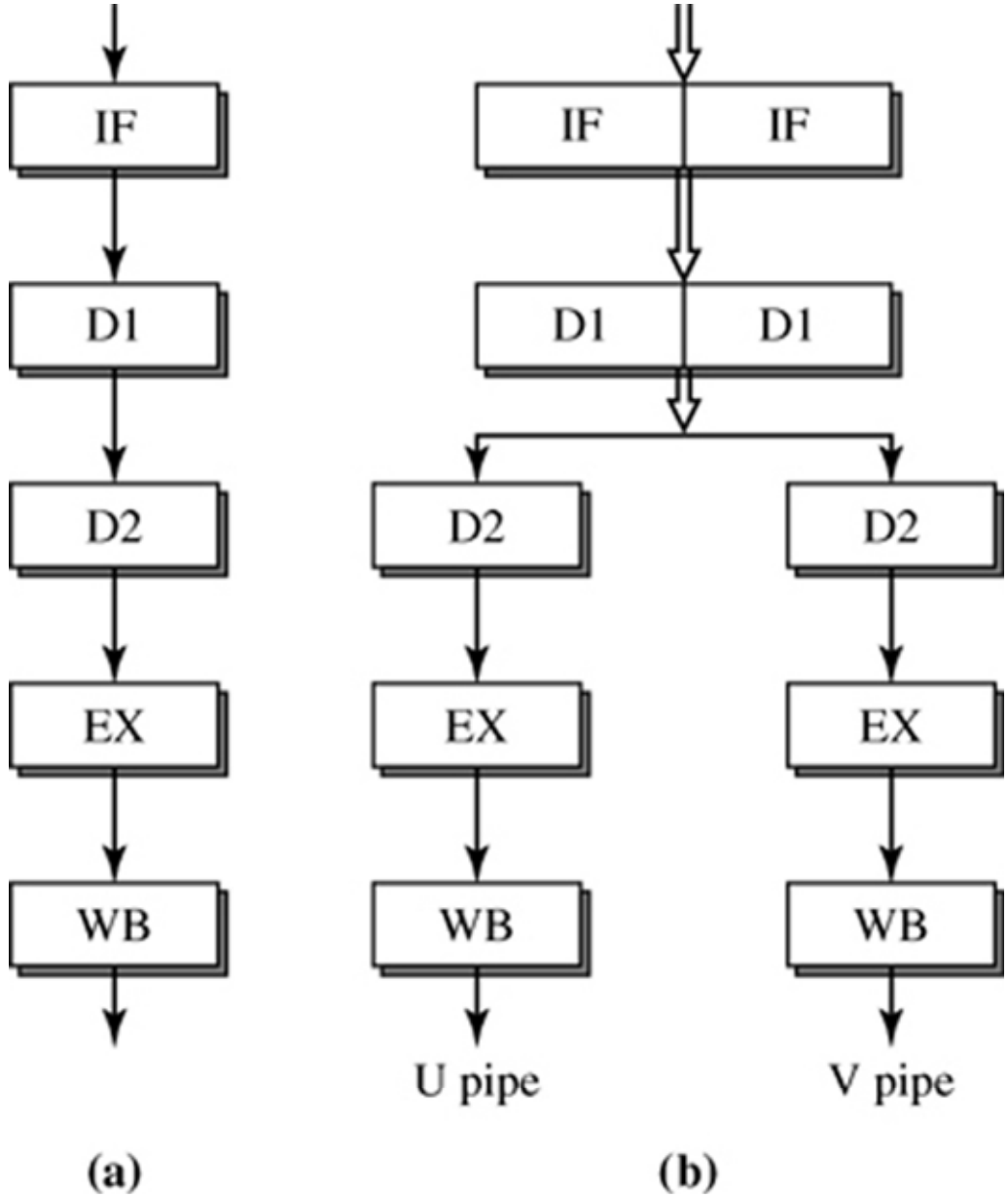

Figure 4.4: (a) The Five-Stage i486 Scalar Pipeline; (b) The Five-Stage Pentium Parallel Pipeline of Width *s*=2.

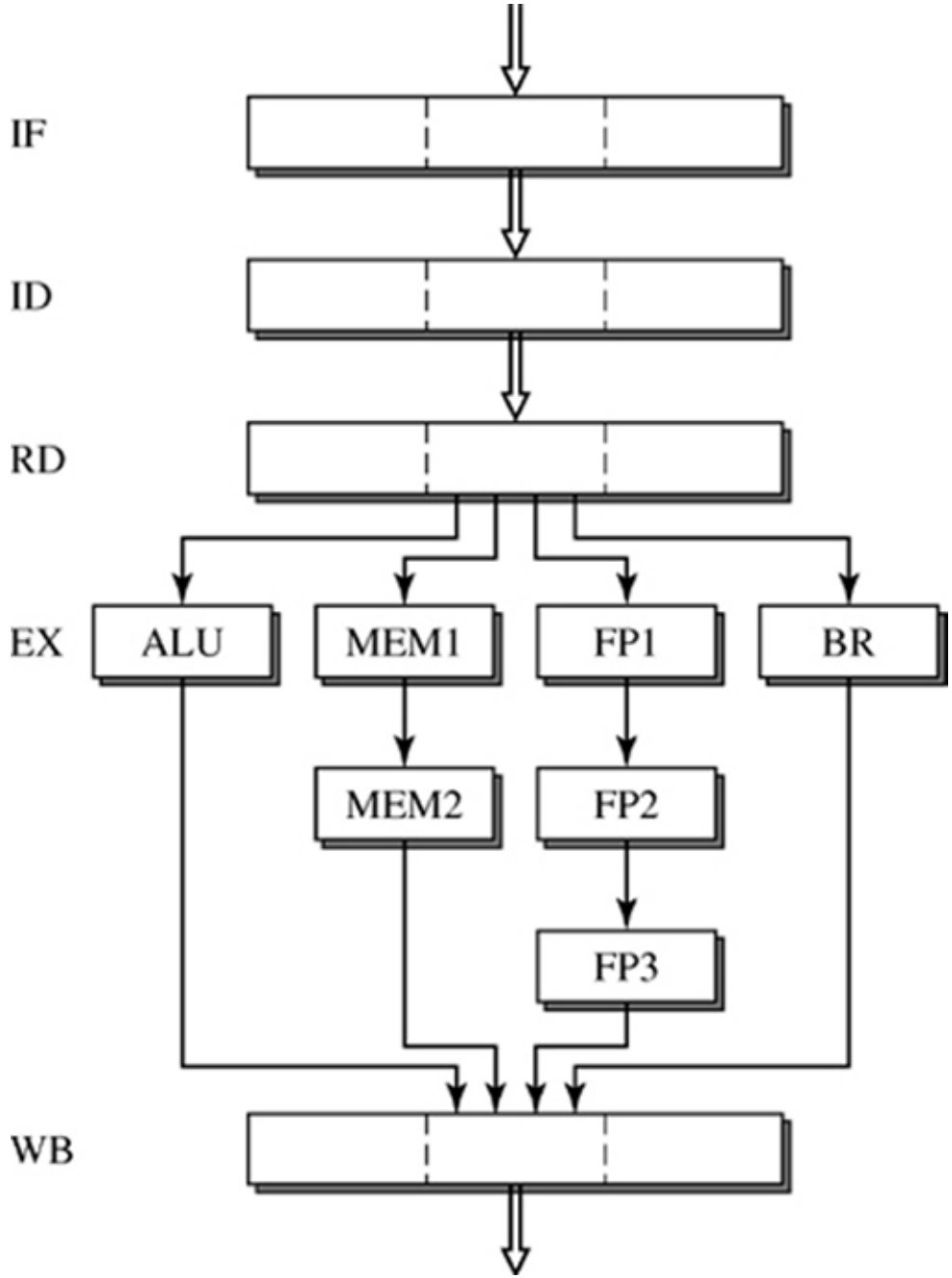

Figure 4.5: A Diversified Parallel Pipeline with Four Execution Pipes.

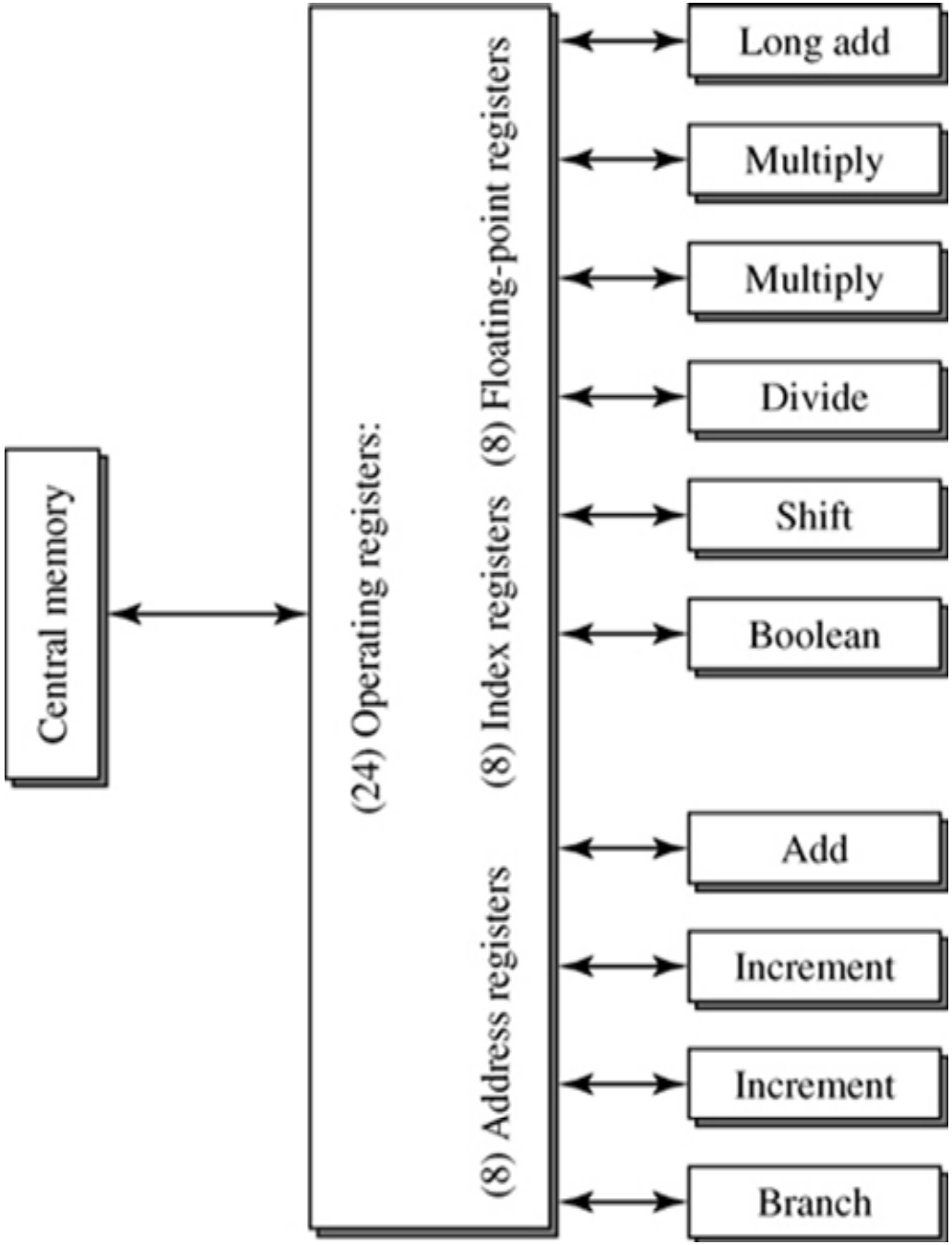

Figure 4.6: The CDC 6600 with 10 Diversified Functional Units in its CPU.

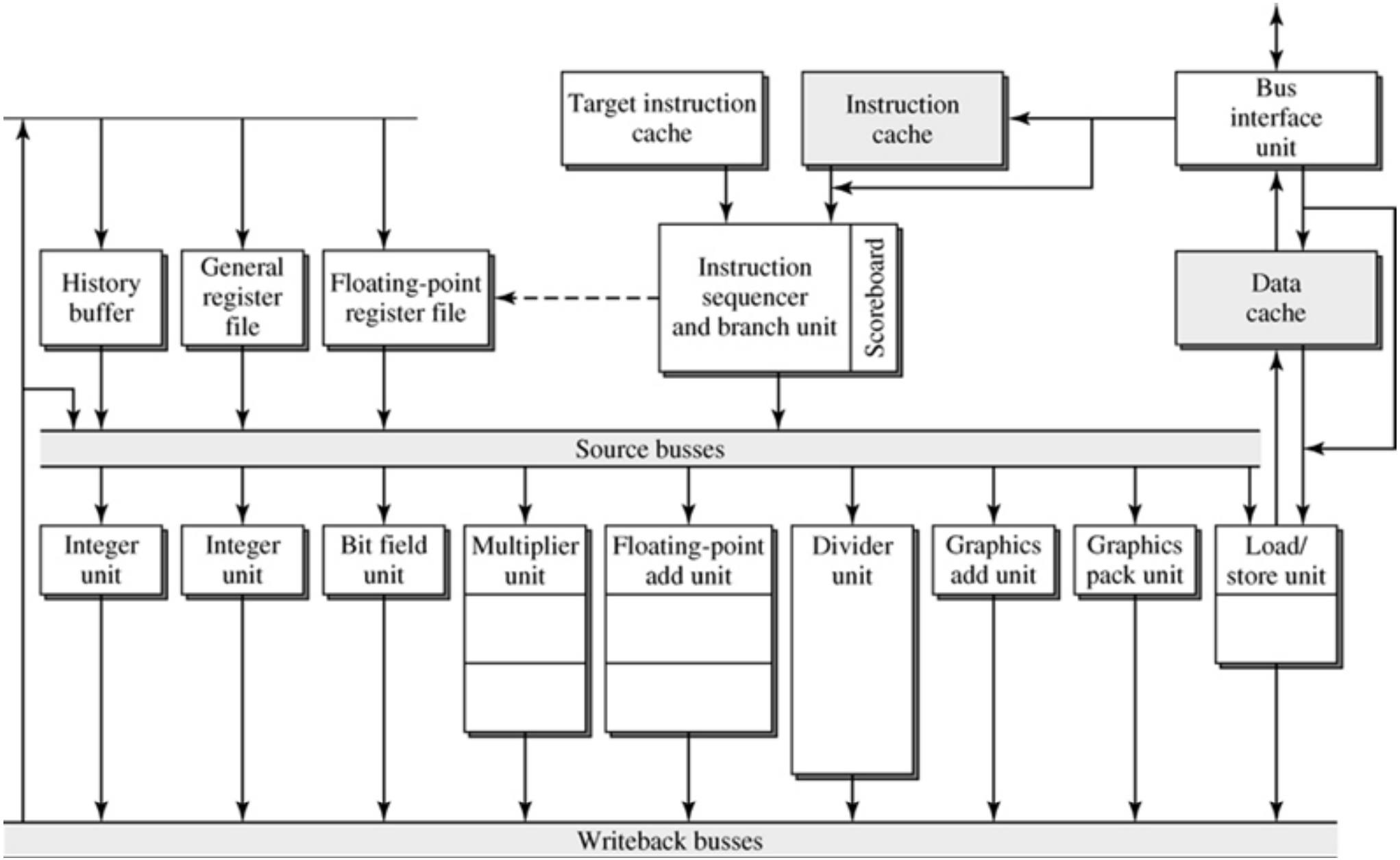

Figure 4.7: The Motorola 88110 Superscalar Microprocessor.
Source: Diefendorf and Allen, 1992.

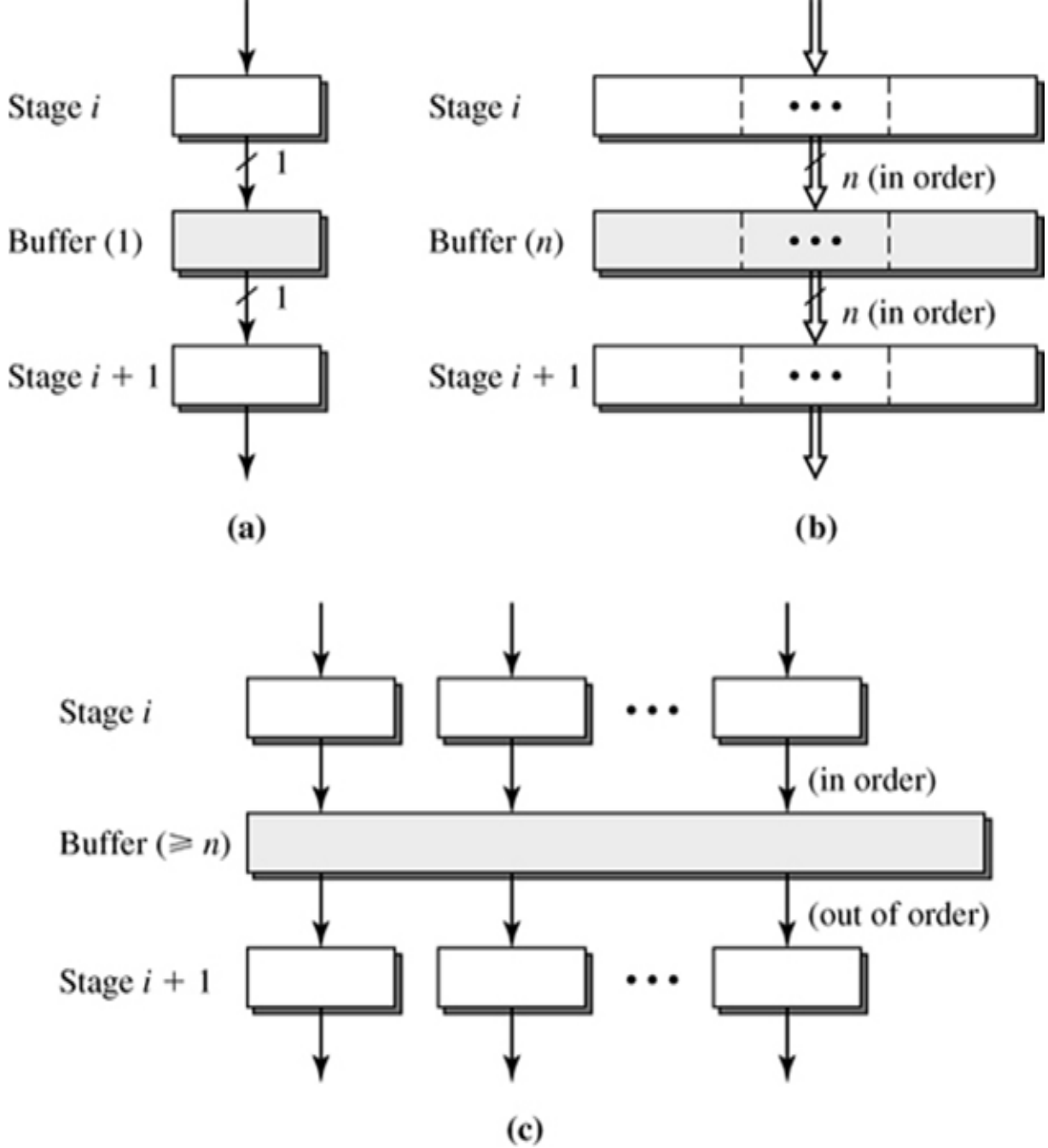

Figure 4.8: Interpipeline-Stage Buffers: (a) Single-Entry Buffer; (b) Multientry Buffer; (c) Multientry Buffer with Reordering.

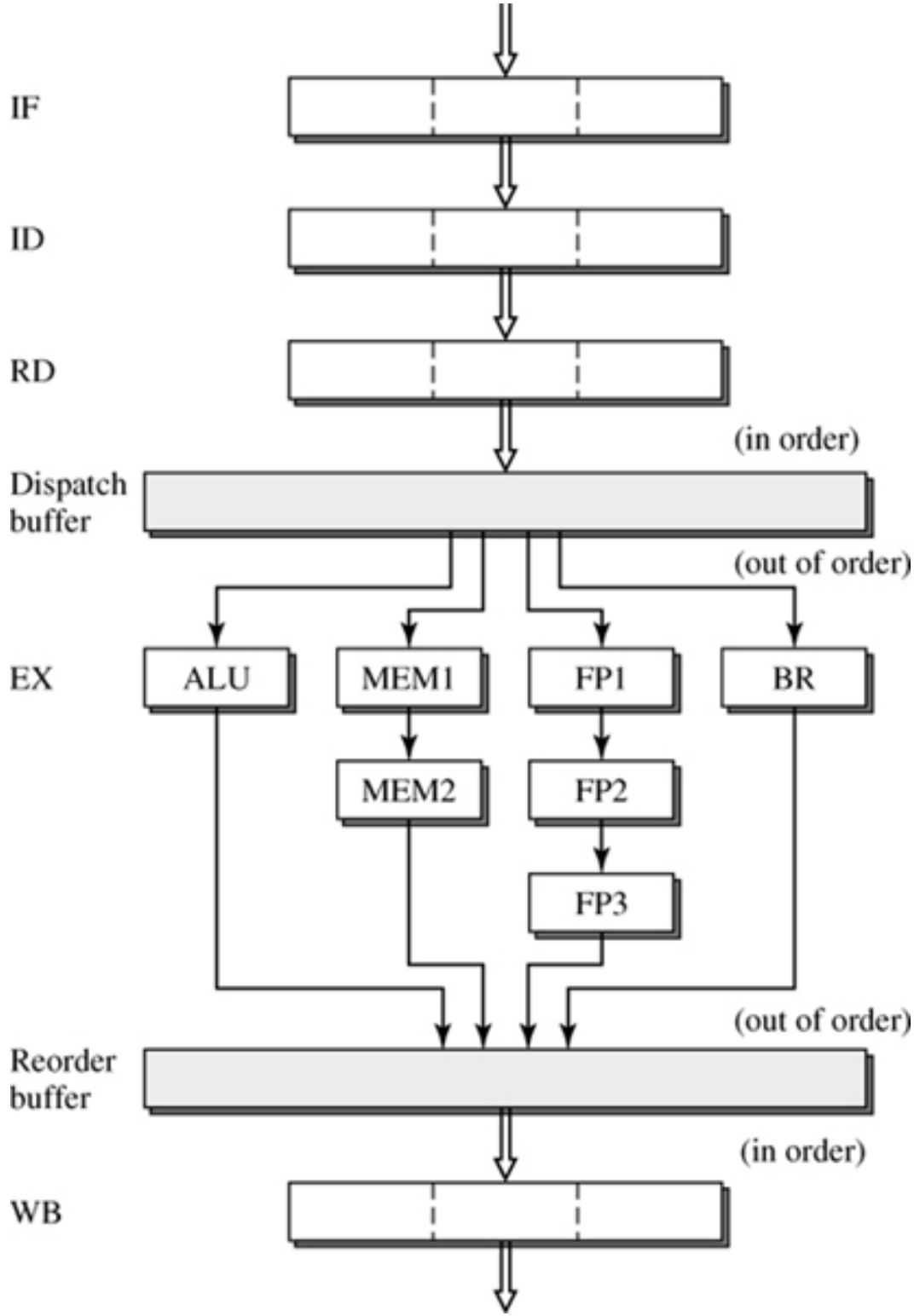

Figure 4.9: A Dynamic Pipeline of Width *s*=3.

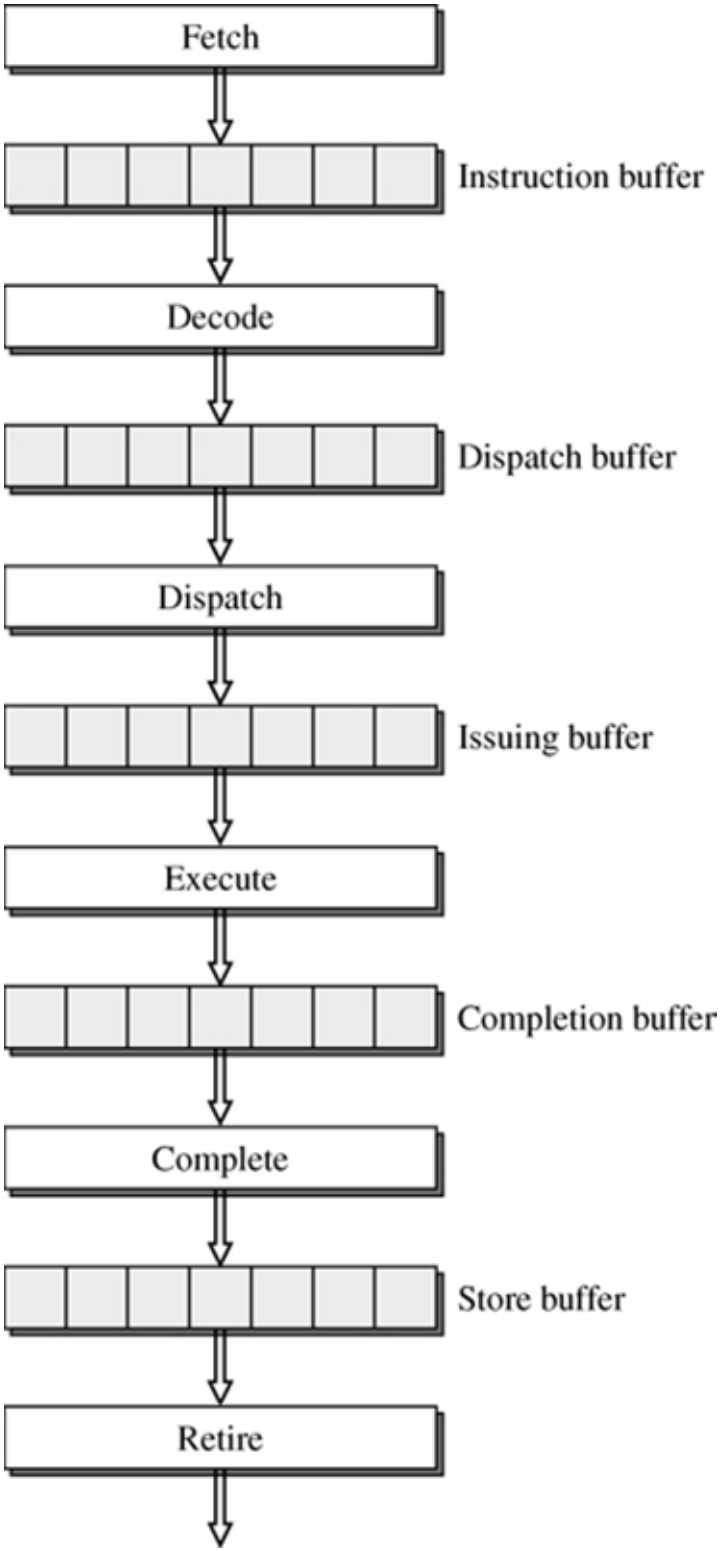

Figure 4.10: The Six-Stage Template (TEM) Superscalar Pipeline.

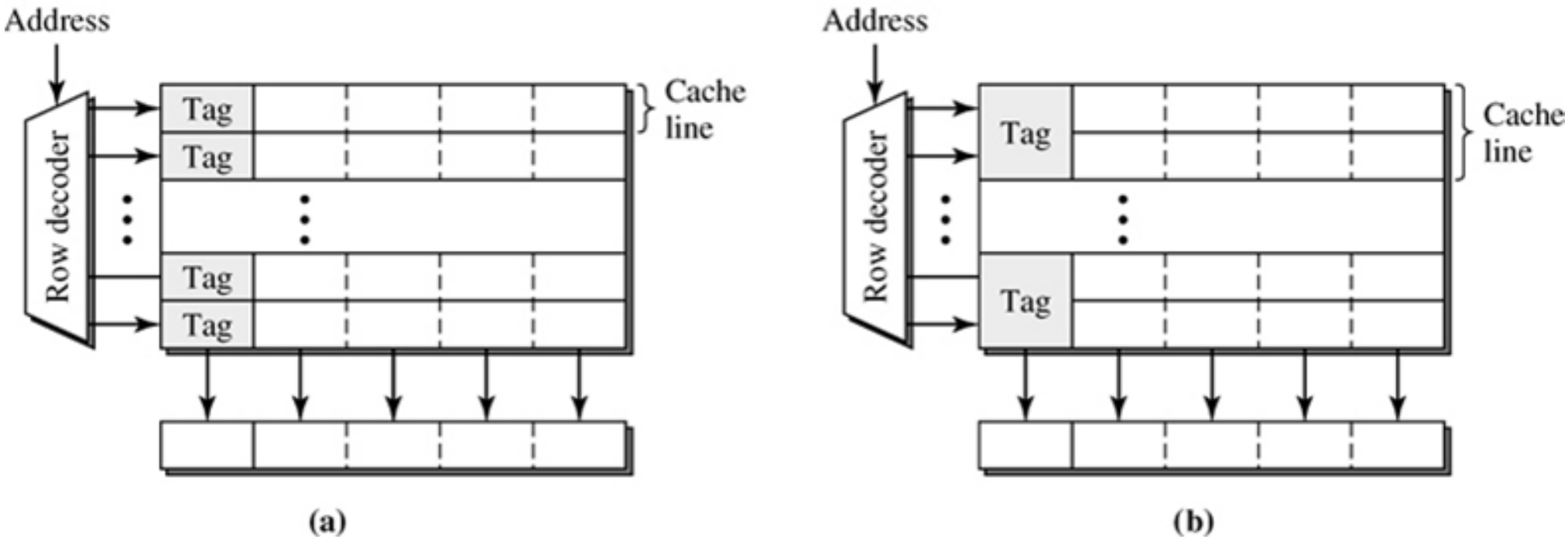

Figure 4.11: Organization of a Wide I-Cache: (a) One Cache Line is Equal to One Physical Row; (b) One Cache Line is Equal to Two Physical Rows.

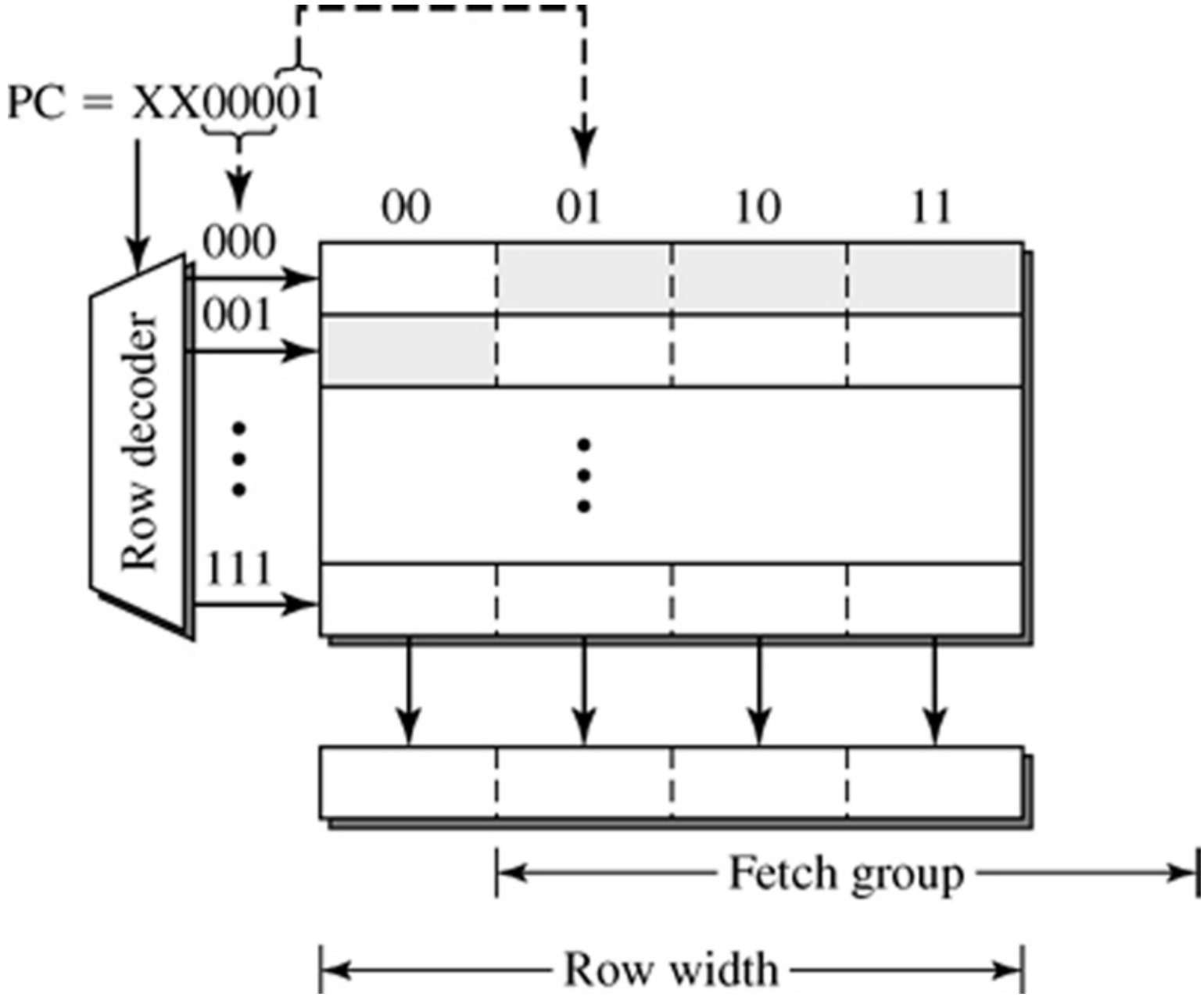

Figure 4.12: Misalignment of the Fetch Group Relative to the Row Boundaries of the I-Cache Array.

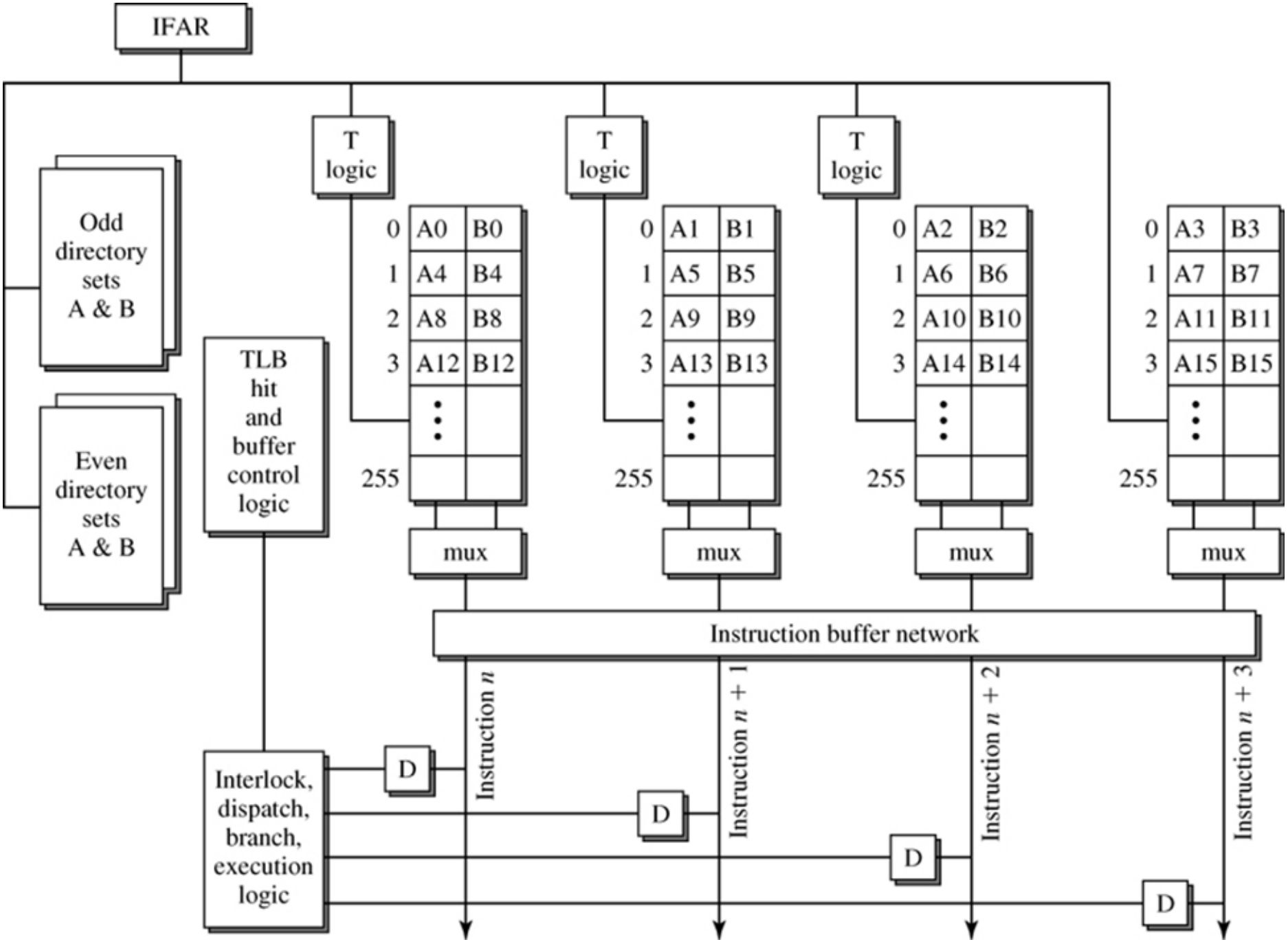

Figure 4.13: Organization of the RS/6000 Two-Way Set-Associative I-Cache with Auto-Realignment.

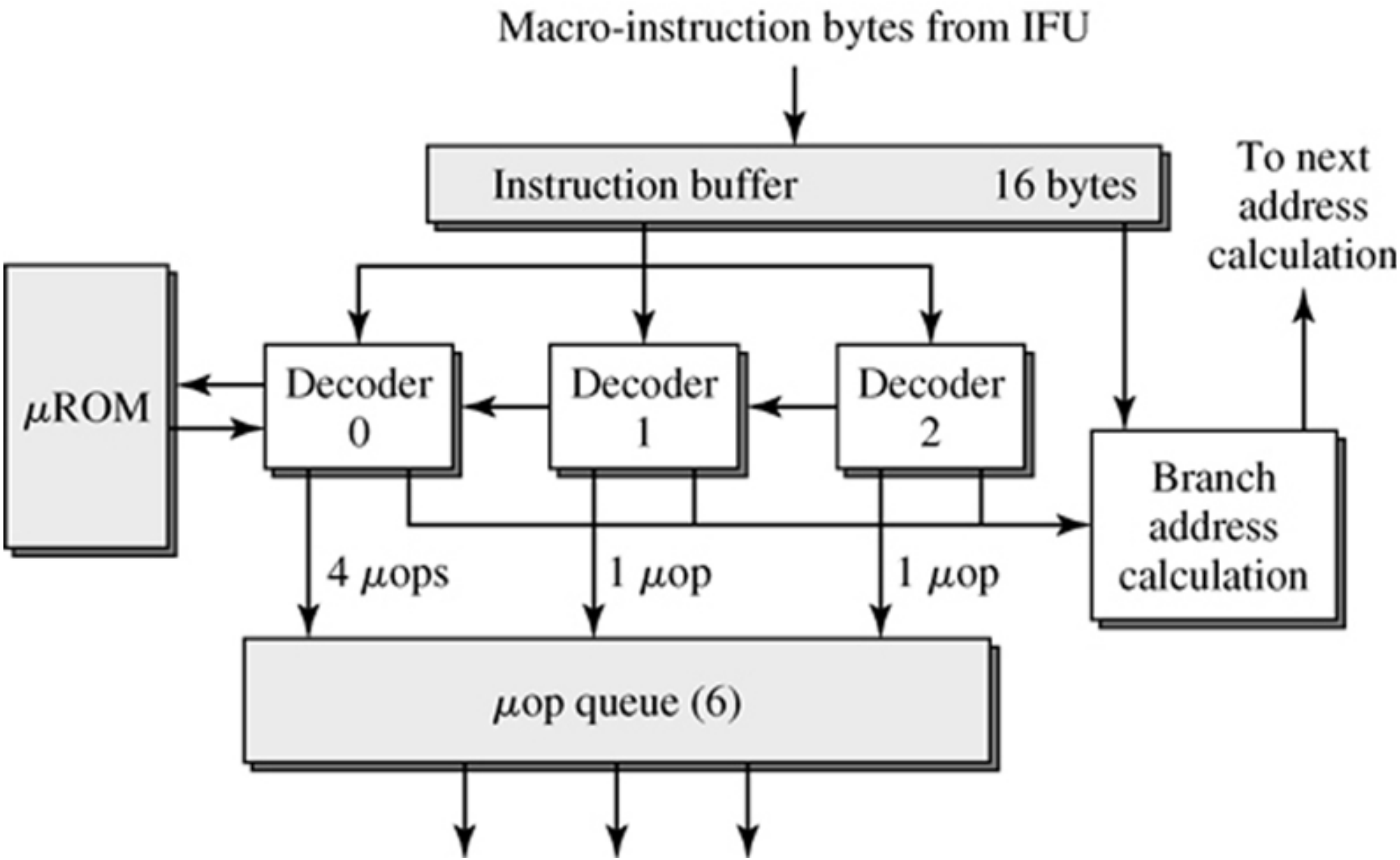

Figure 4.14: The Fetch/Decode Unit of the Intel P6 Superscalar Pipeline.

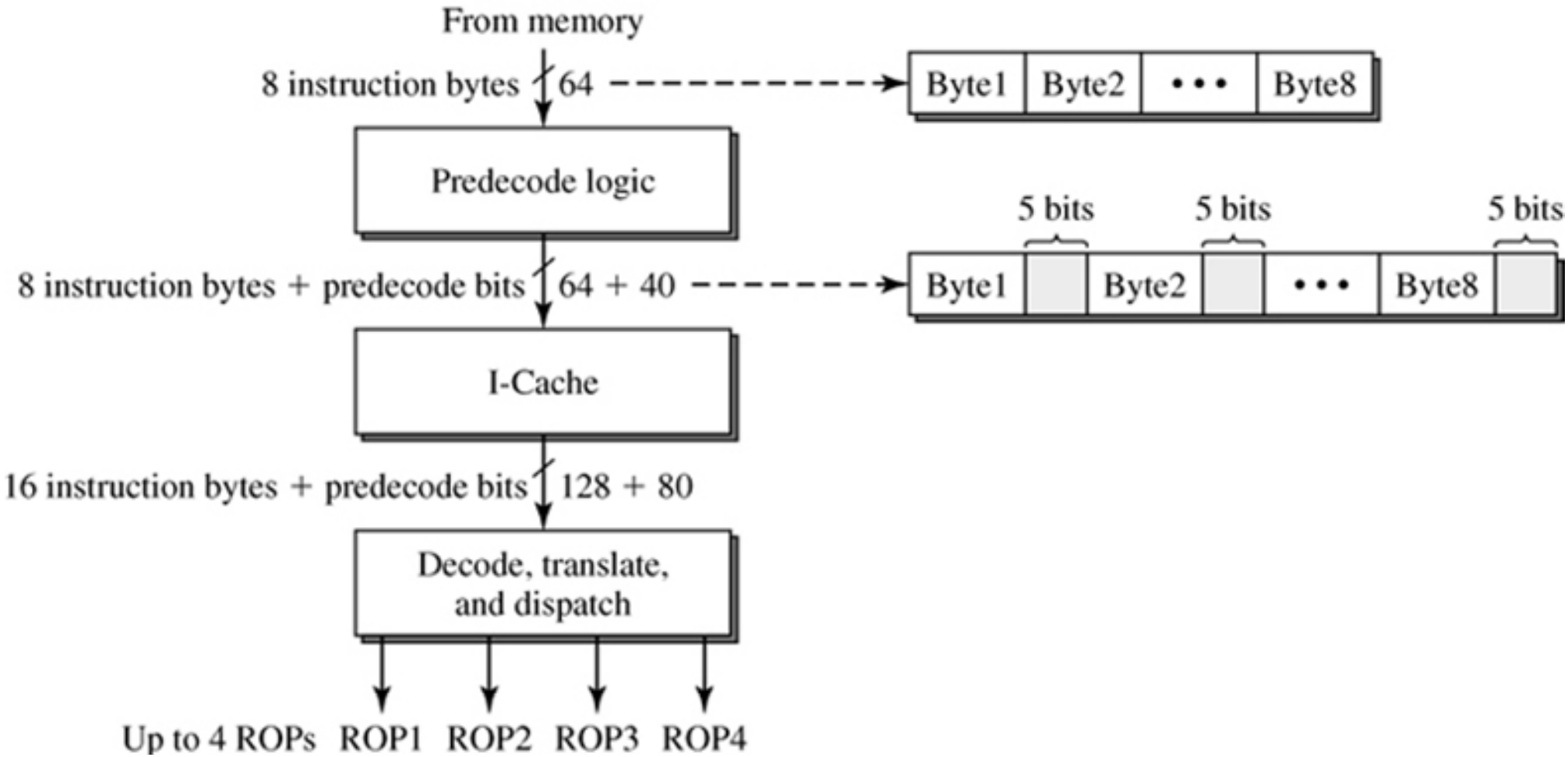

Figure 4.15: The Predecoding Mechanism of the AMD K5.

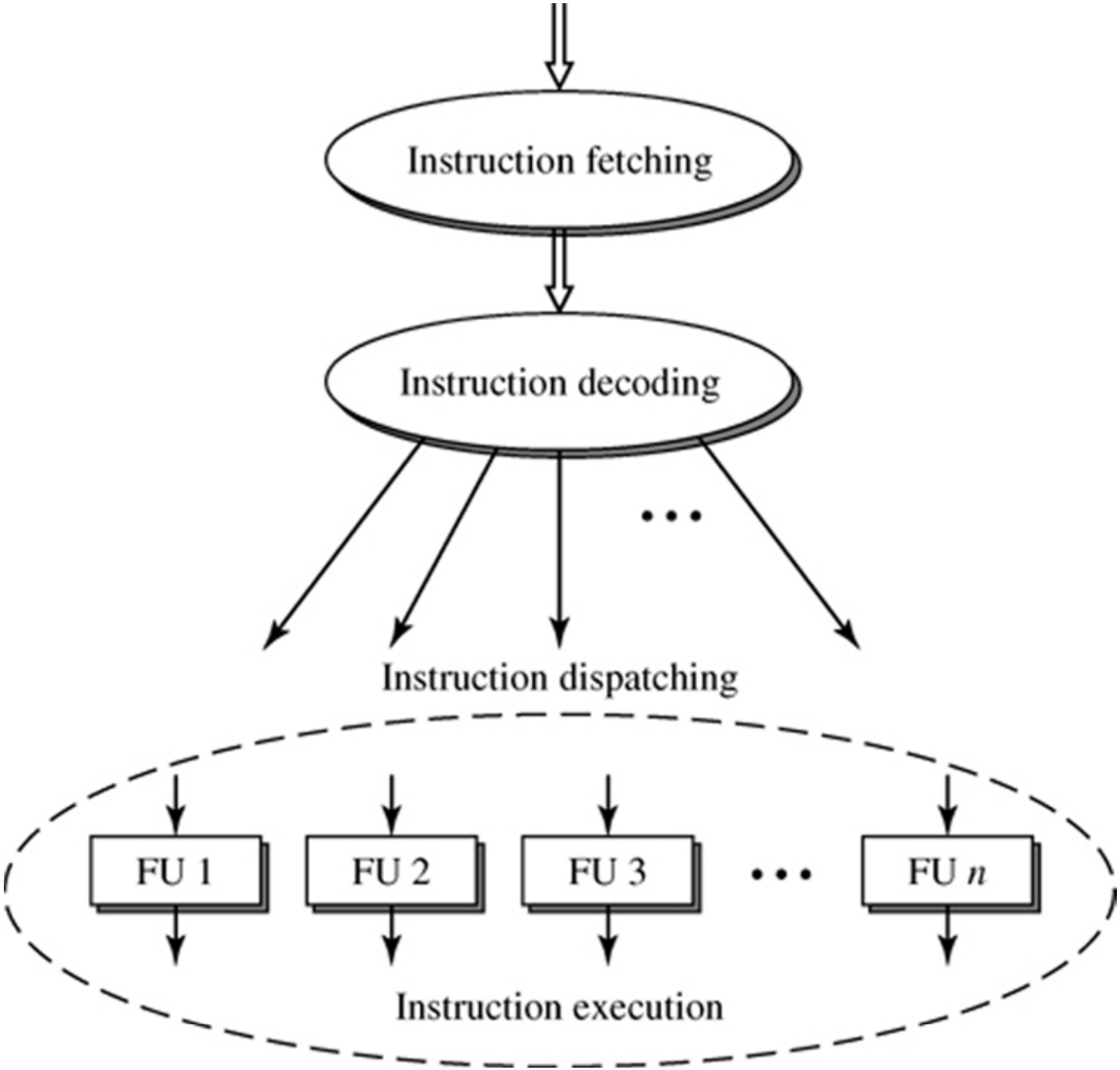

Figure 4.16: The Necessity of Instruction Dispatching in a Superscalar Pipeline.

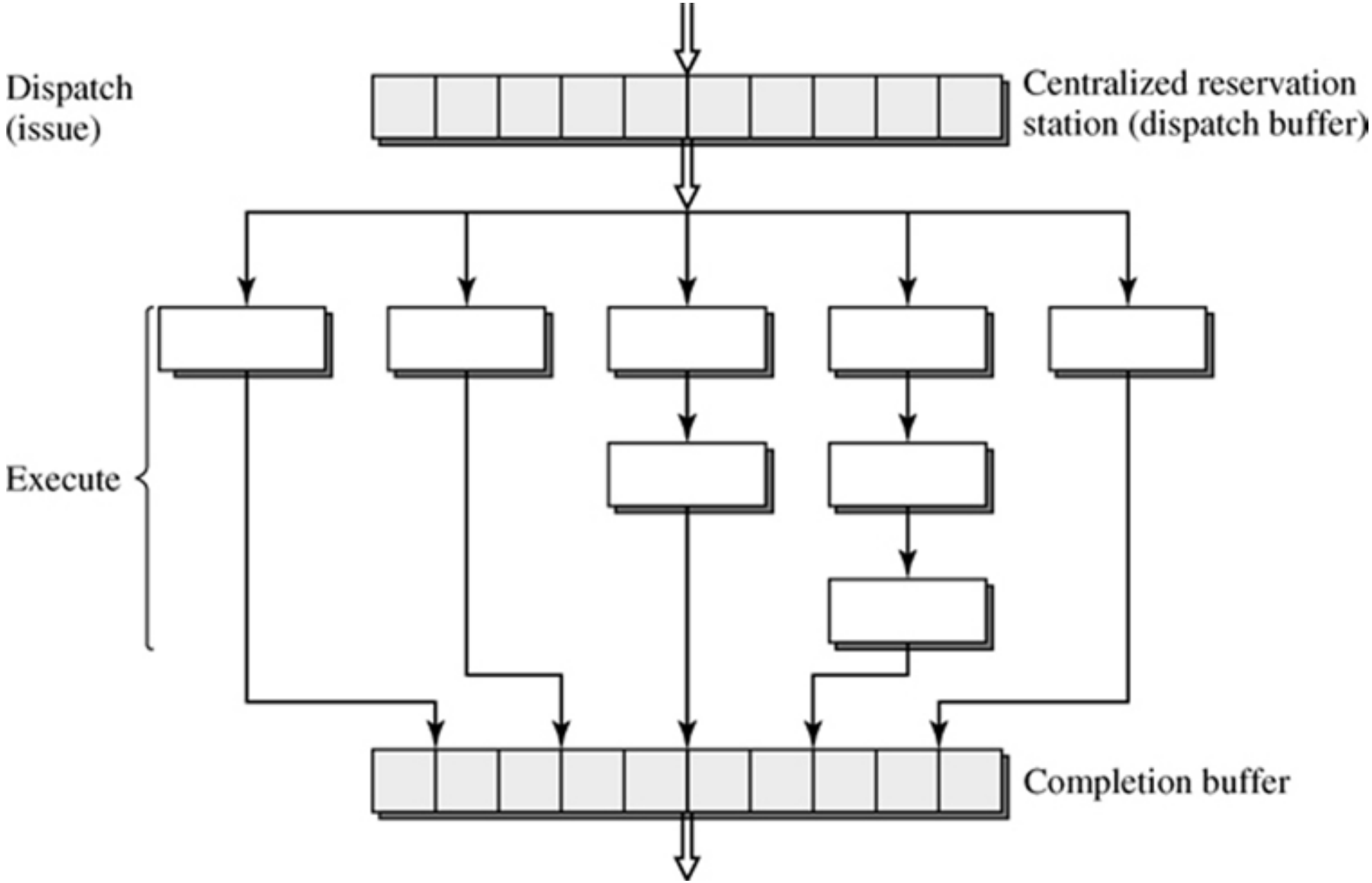

Figure 4.17: Centralized Reservation Station.

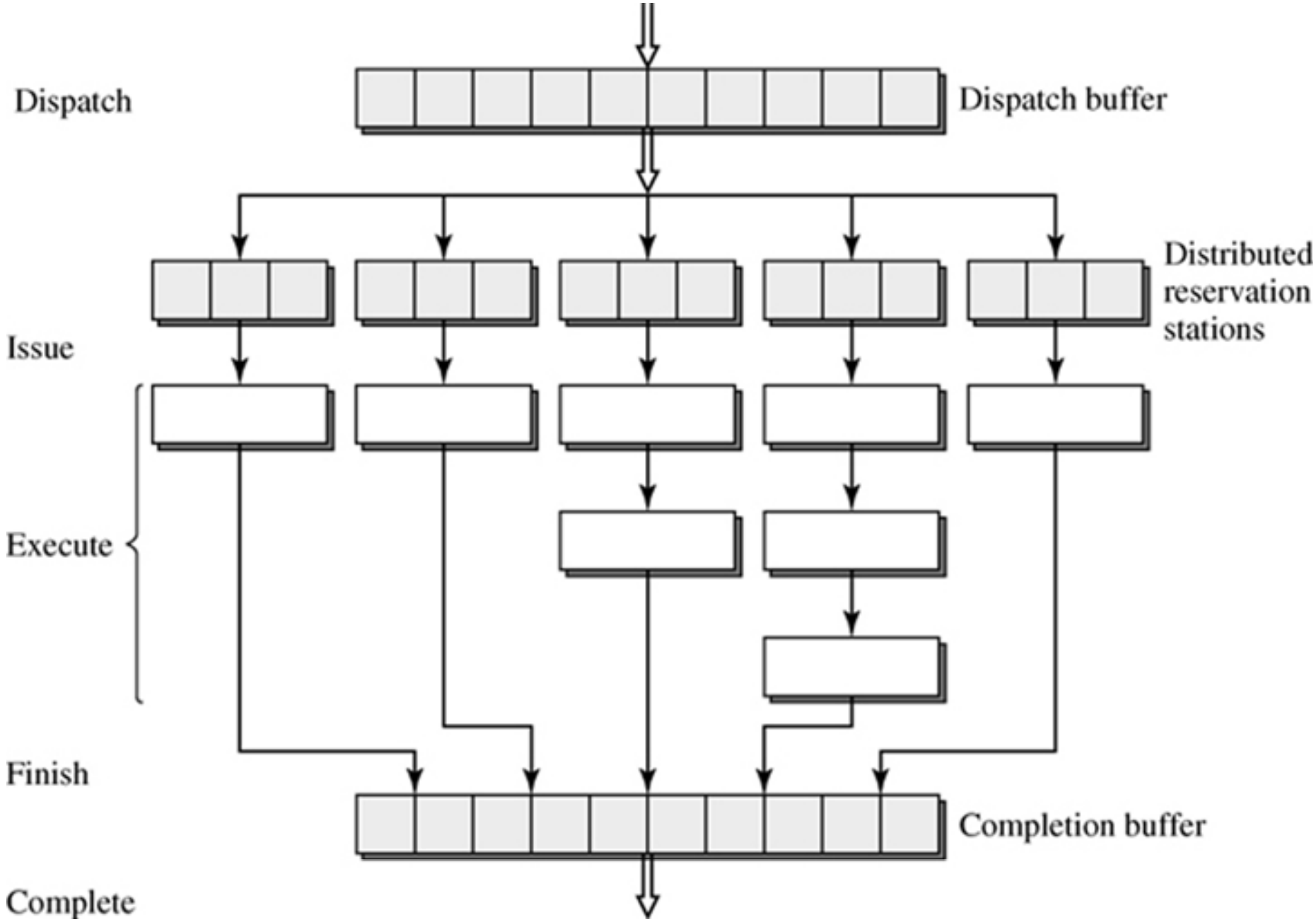

Figure 4.18: Distributed Reservation Stations.

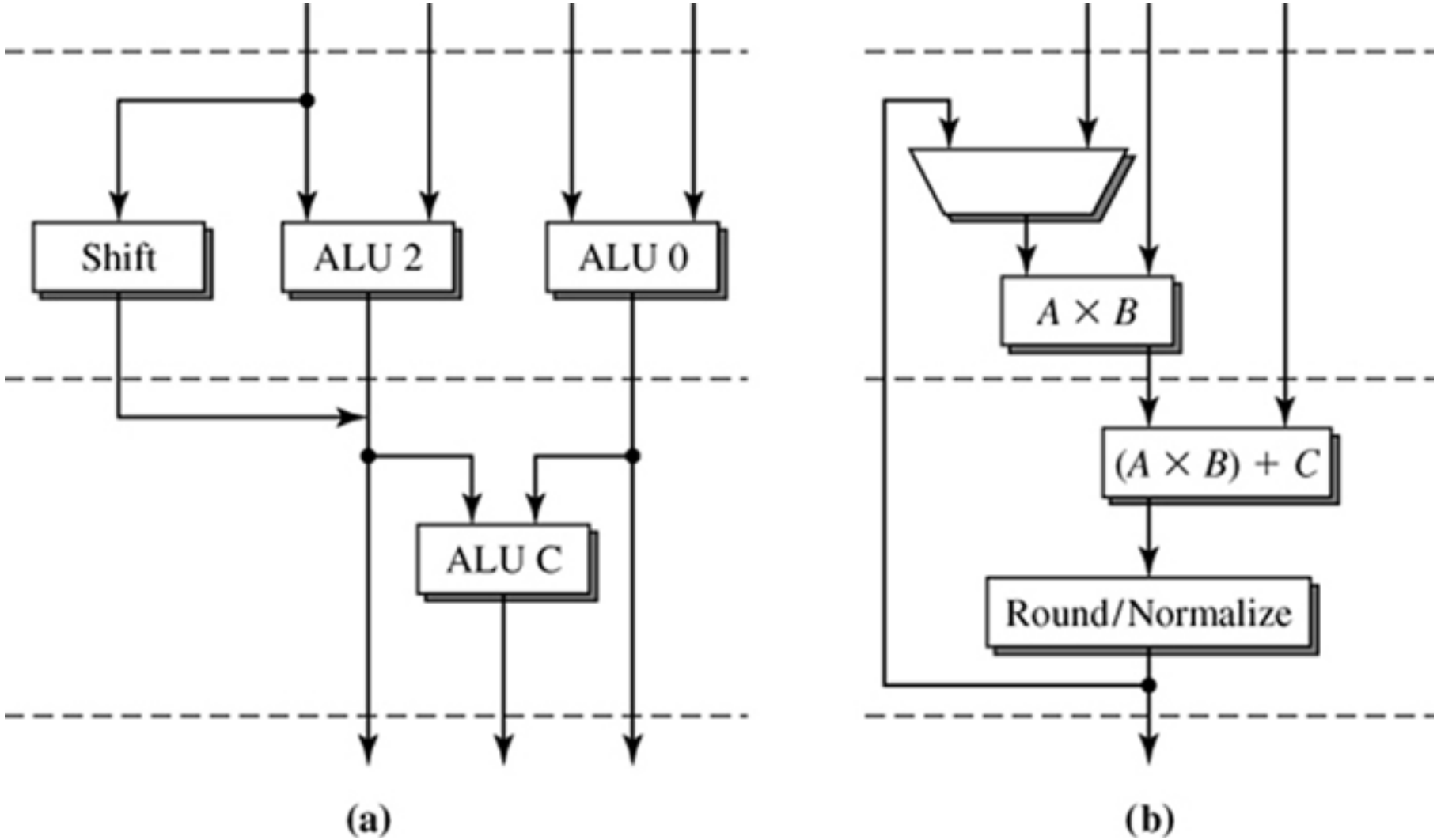

Figure 4.19: (a) Integer Functional Unit in the TI SuperSPARC; (b) Floating-Point Unit in the IBM RS/6000.

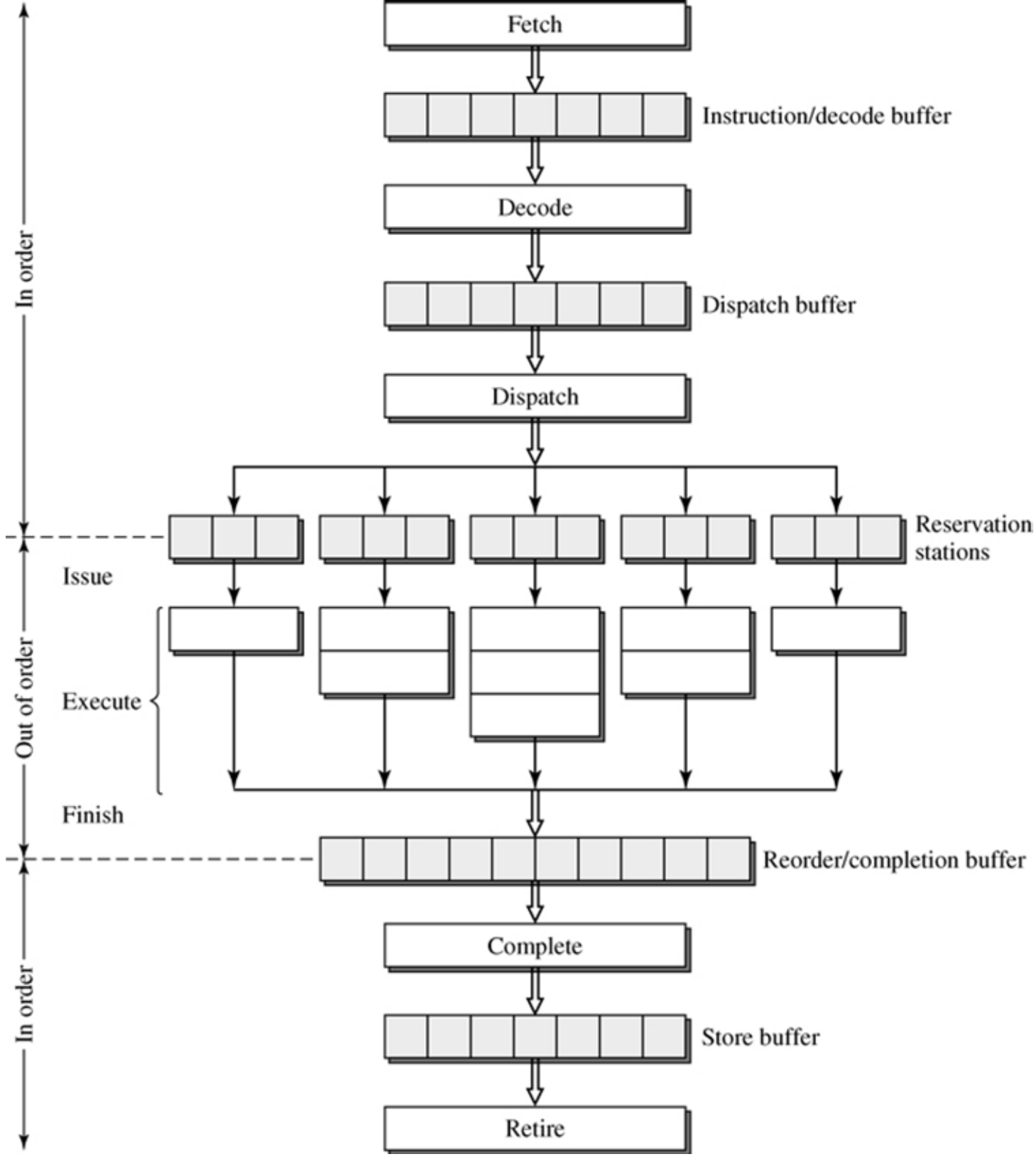

Figure 4.20: A Dynamic Pipeline with Reservation Station and Reorder Buffer.