

Figure 6.1: Block Diagram of the PowerPC 620 Microprocessor.

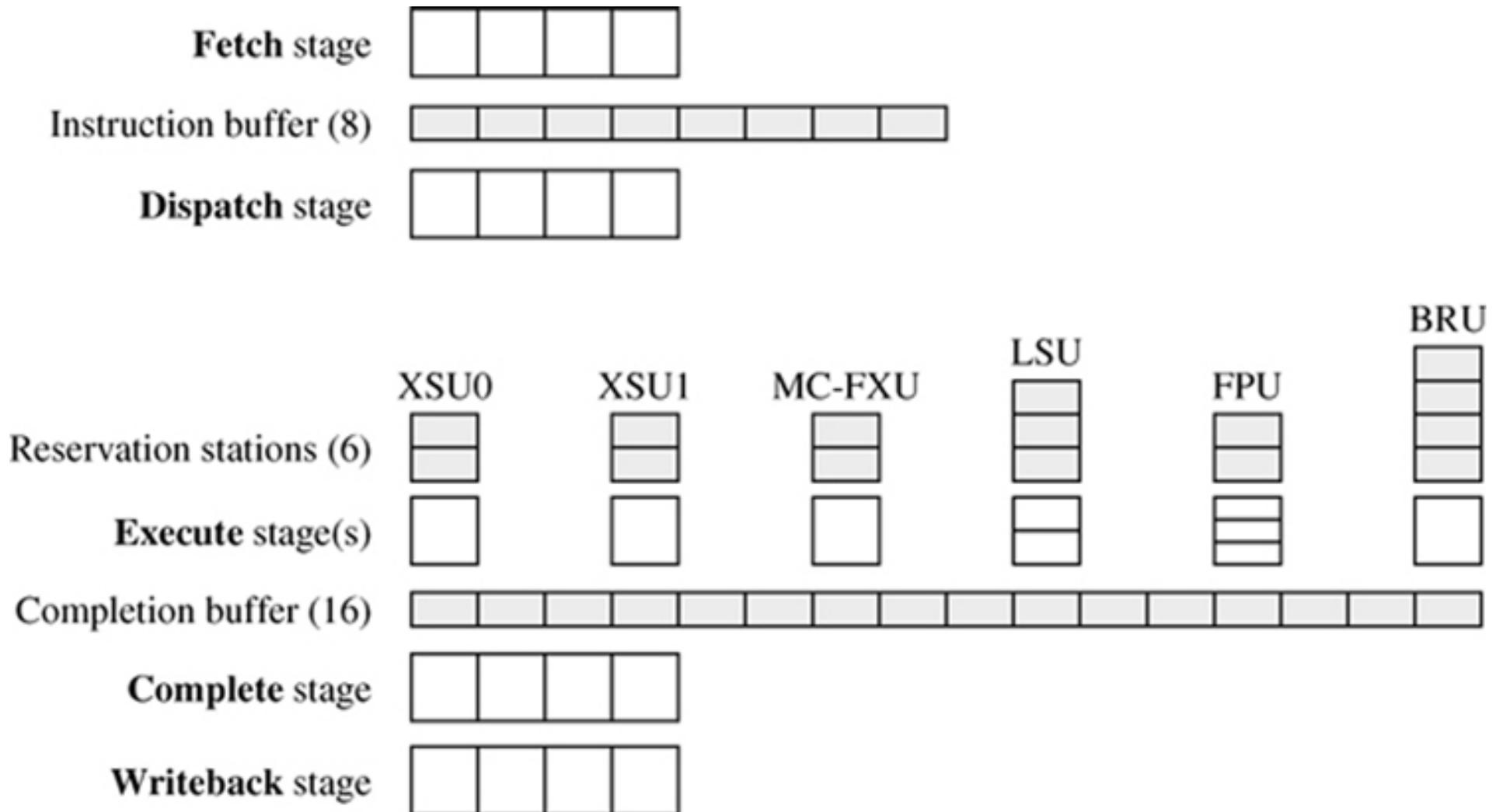


Figure 6.2: Instruction Pipeline of the PowerPC 620 Microprocessor.

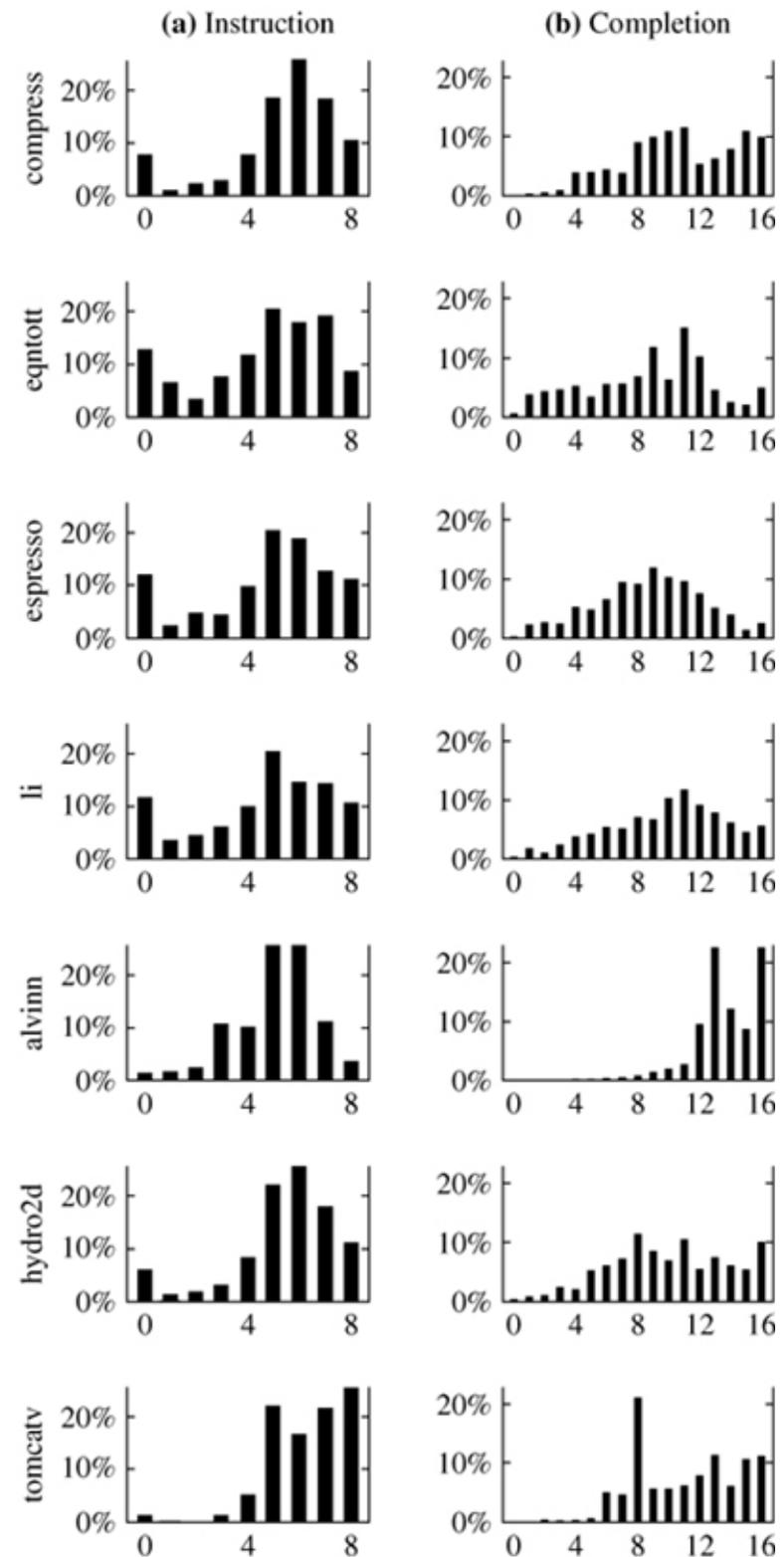


Figure 6.3: Profiles of the (a) Instruction Buffer and (b) Completion Buffer Utilizations.

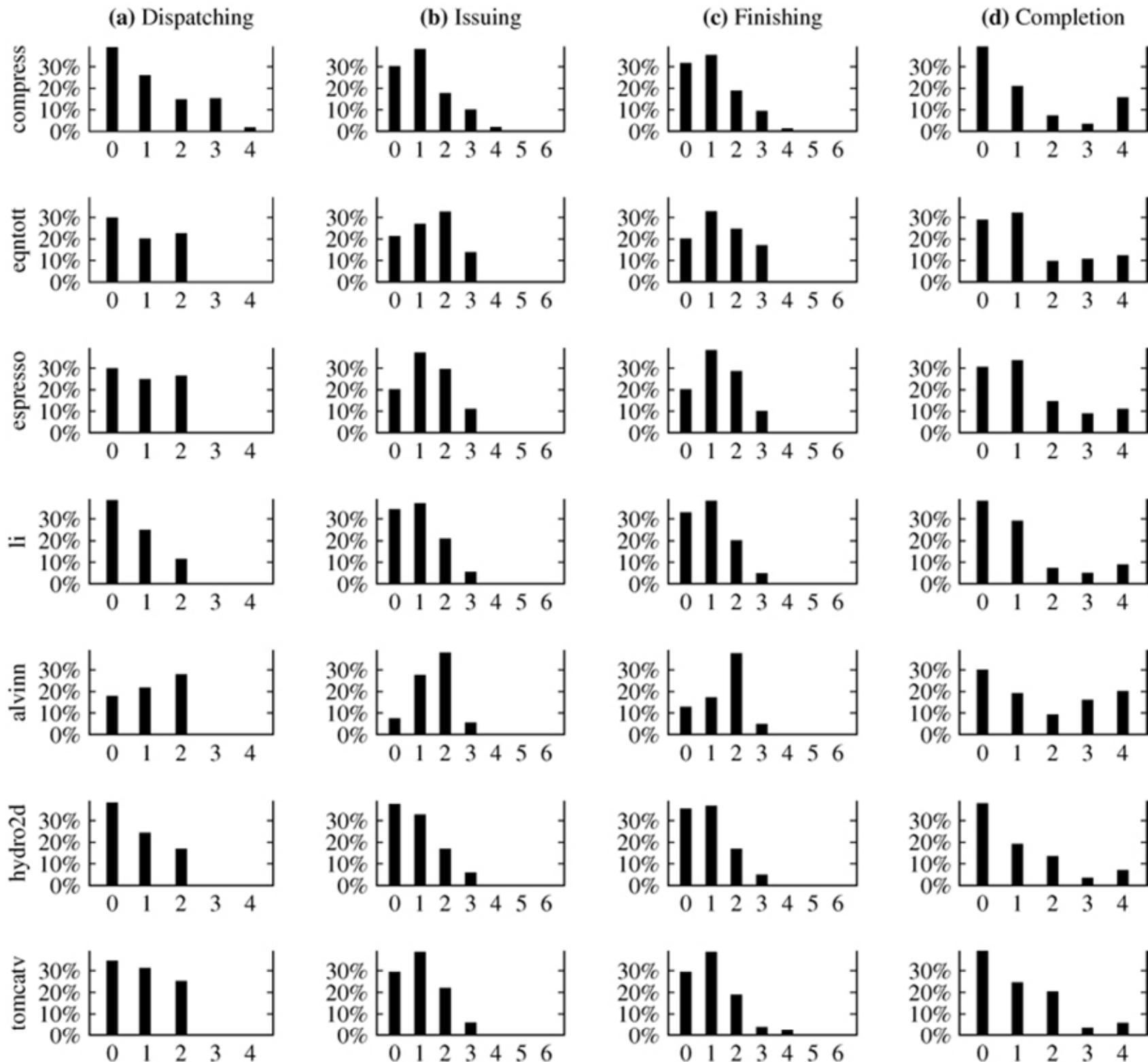


Figure 6.4:
Distribution of
the Instruction
(a) Dispatching,
(b) Issuing, (c)
Finishing, and
(d) Completion
Parallelisms.

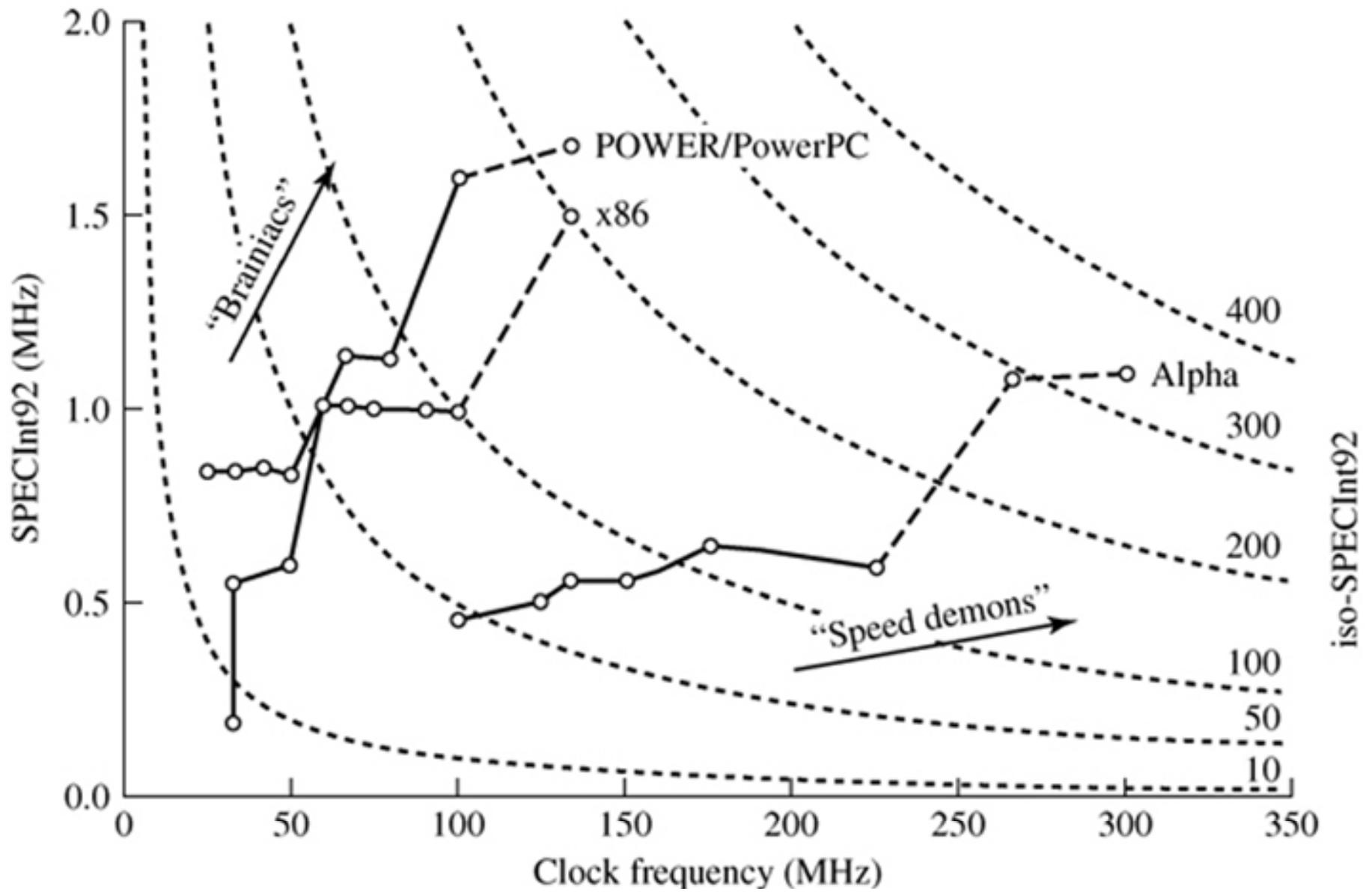


Figure 6.5: Evolution of Superscalar Families.

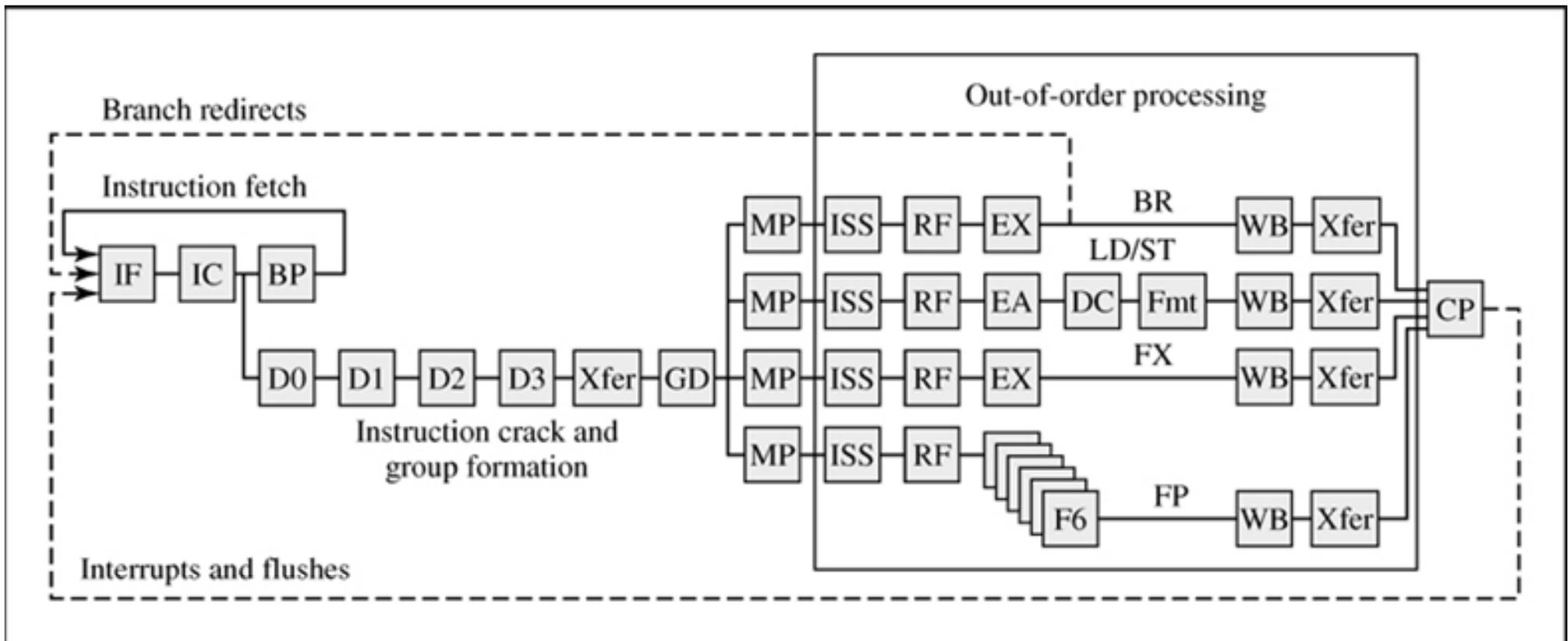


Figure 6.6: POWER4 Pipeline Structure.

Source: Tendler et al., 2001.