

Figure 7.1: P6 Microarchitecture Block Diagram

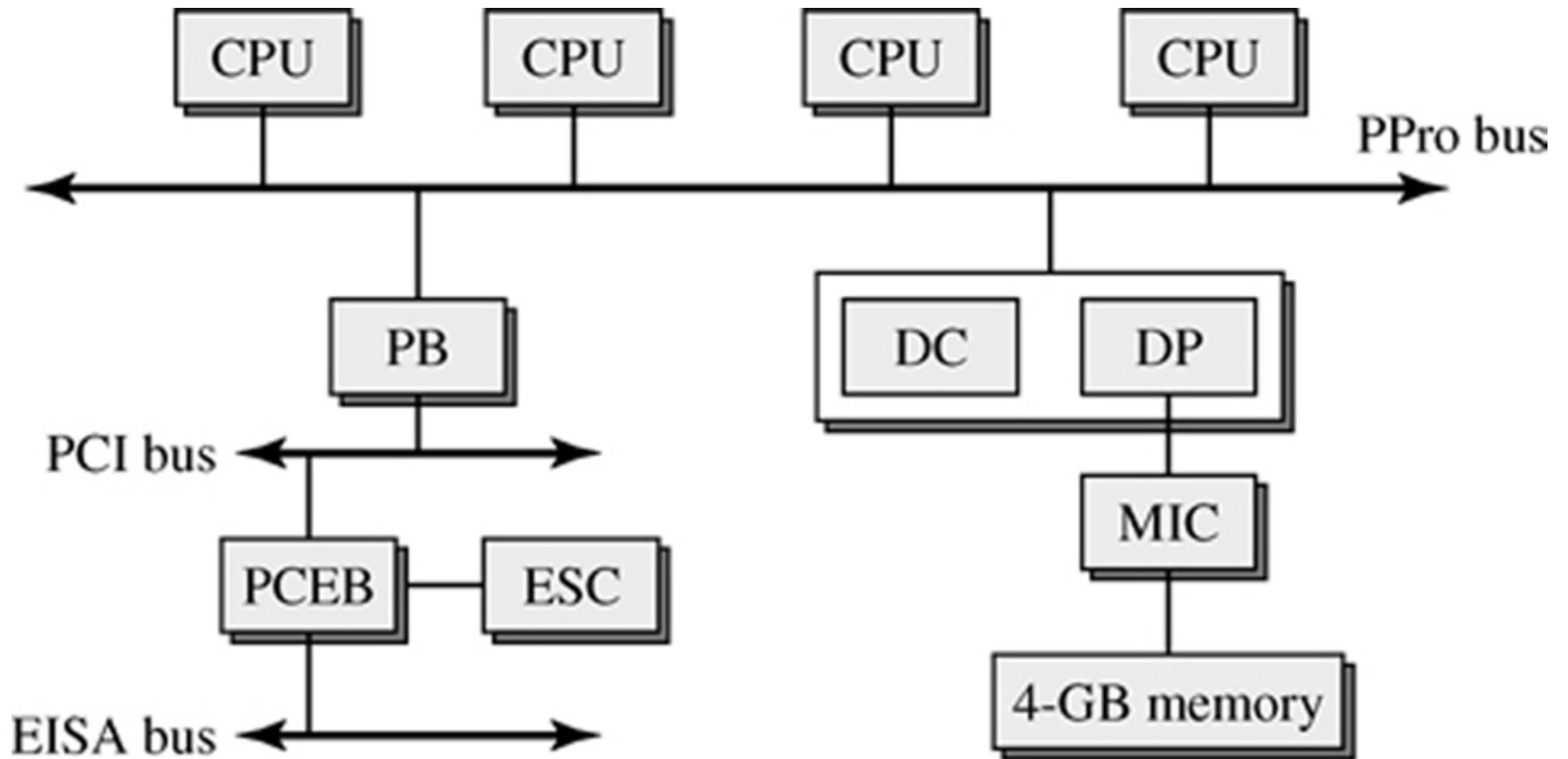


Figure 7.2: P6 Pentium Pro System Block Diagram.

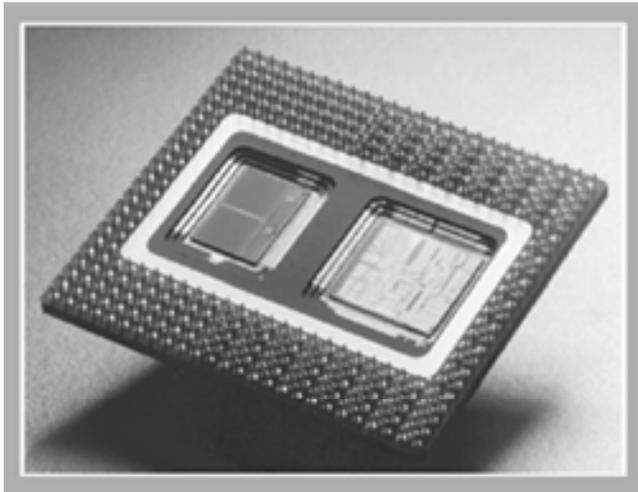


Figure 7.3: P6 Product Packaging.

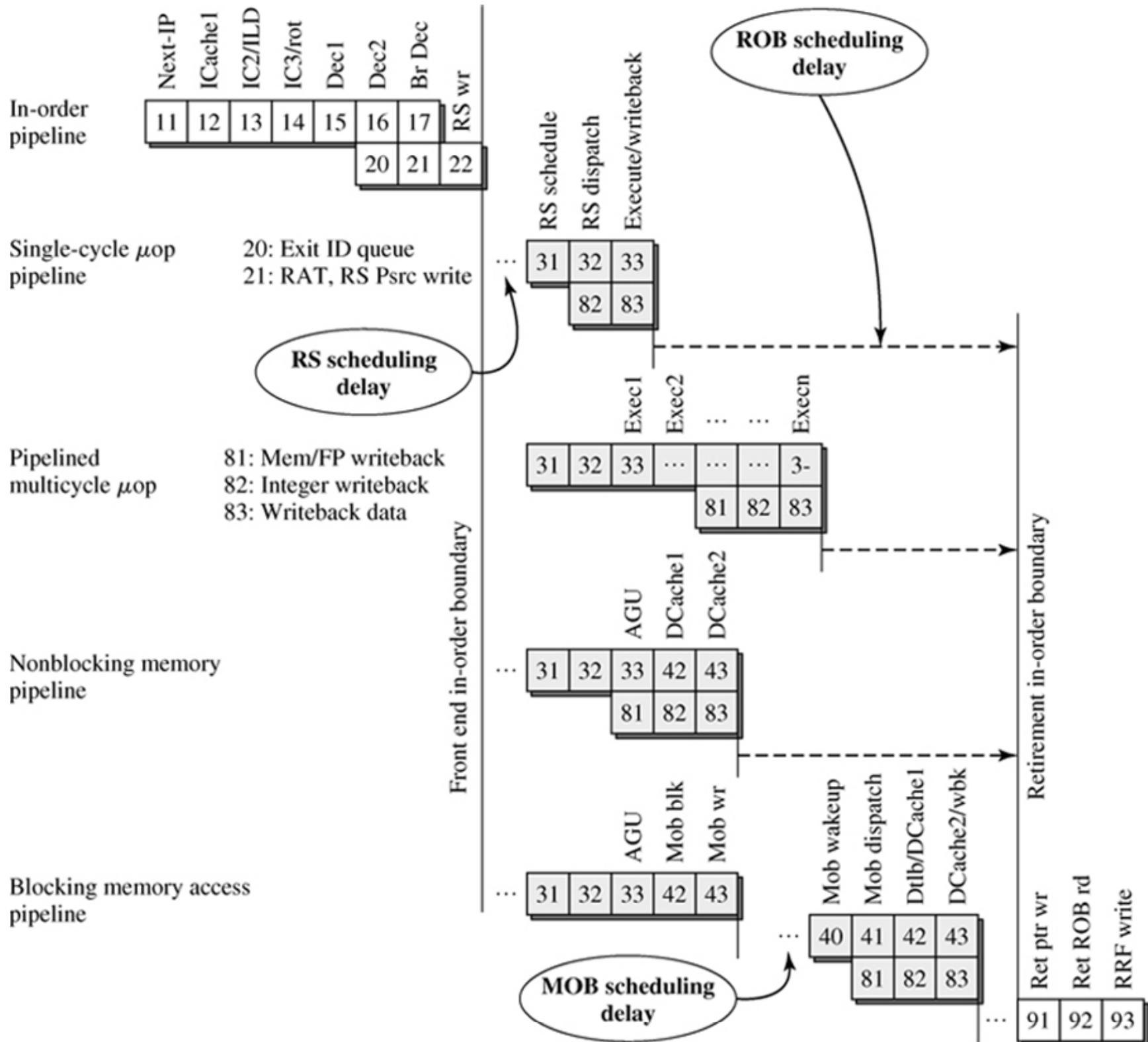
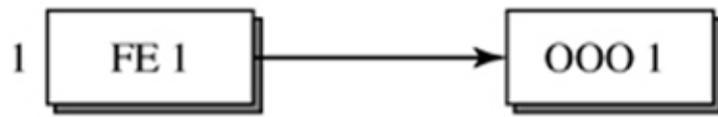
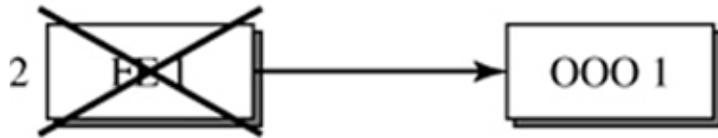


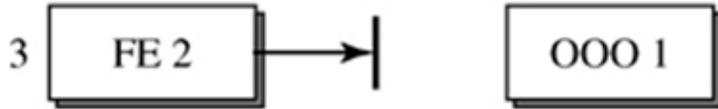
Figure 7.4:  
P6  
Pipelining.



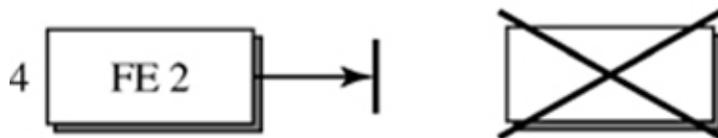
Normal operation, front end speculatively fetching and decoding IA-32 instrs, renaming, and streaming  $\mu$ ops into out-of-order (OOO) core.



OOO core detects mispredicted branch, instructs front end to flush and begin refetching. OOO core continues executing and retiring  $\mu$ ops that were ahead of the mispredicted branch, until core drains.



Front end has flushed, refetched from corrected branch target. New  $\mu$ op stream has now propagated through rename, ready to enter OOO core. But core hasn't finished all  $\mu$ ops present when bad branch was detected. Stall front end, continue draining OOO core.



OOO core has drained; retire bad branch, flush rest of OOO core.



Normal operation, front end speculatively fetching and decoding IA-32 instrs, renaming, and streaming  $\mu$ ops into the out-of-order core.

Figure 7.5: Branch Misspeculation Recovery.

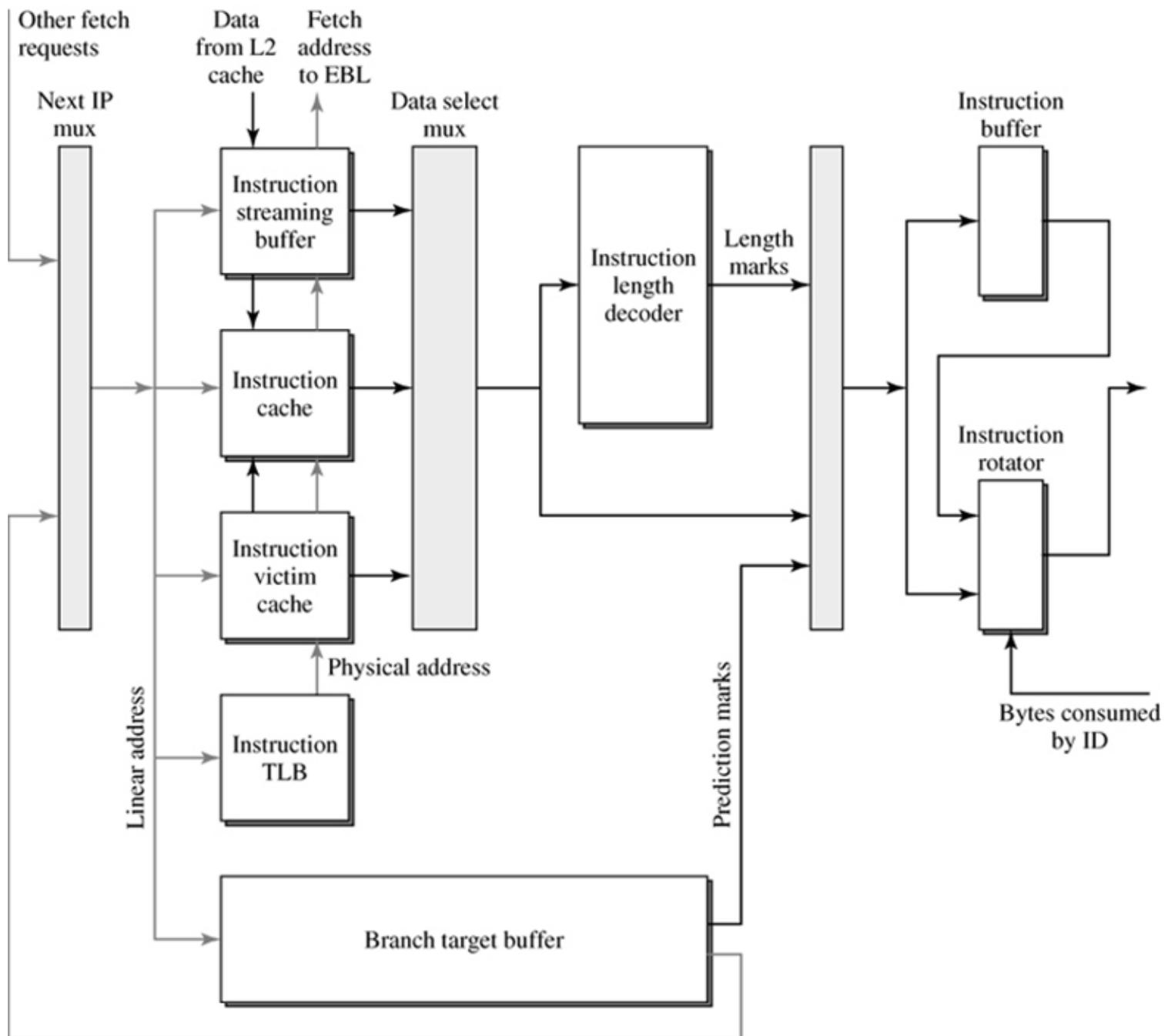


Figure 7.6: Front-End Pipe Staging.

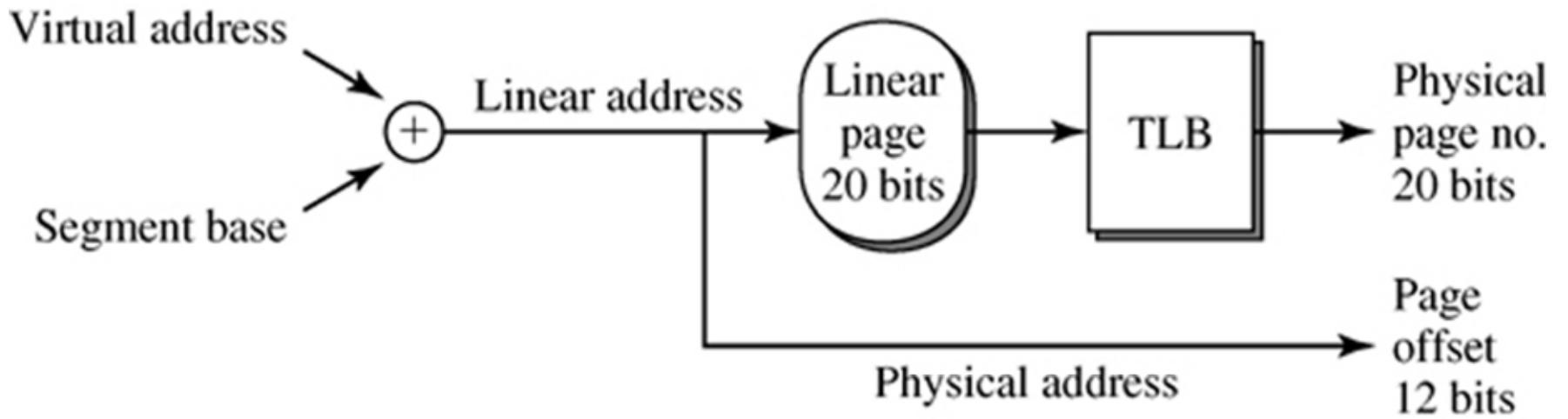
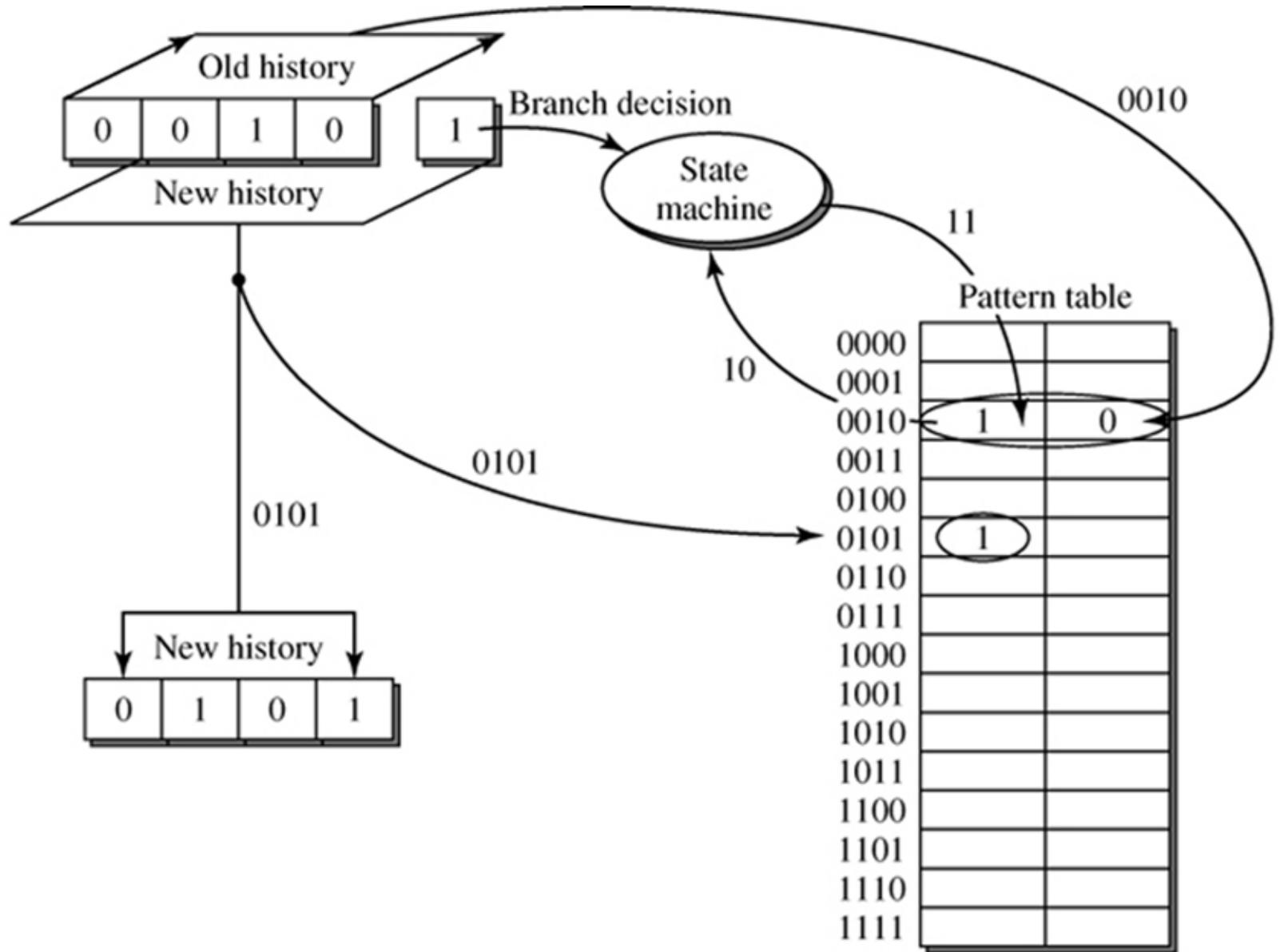


Figure 7.7: Virtual to Linear to Physical Addresses.



Two processes occur in parallel:

1. The new history is used to access the pattern table to get the new prediction bit. This prediction bit is written into the BTB in the next phase.
2. The old history is used to access the pattern table to get the state that has to be updated. The updated state is then written back to the pattern table.

Figure 7.8:  
Yeh's  
Algorithm.



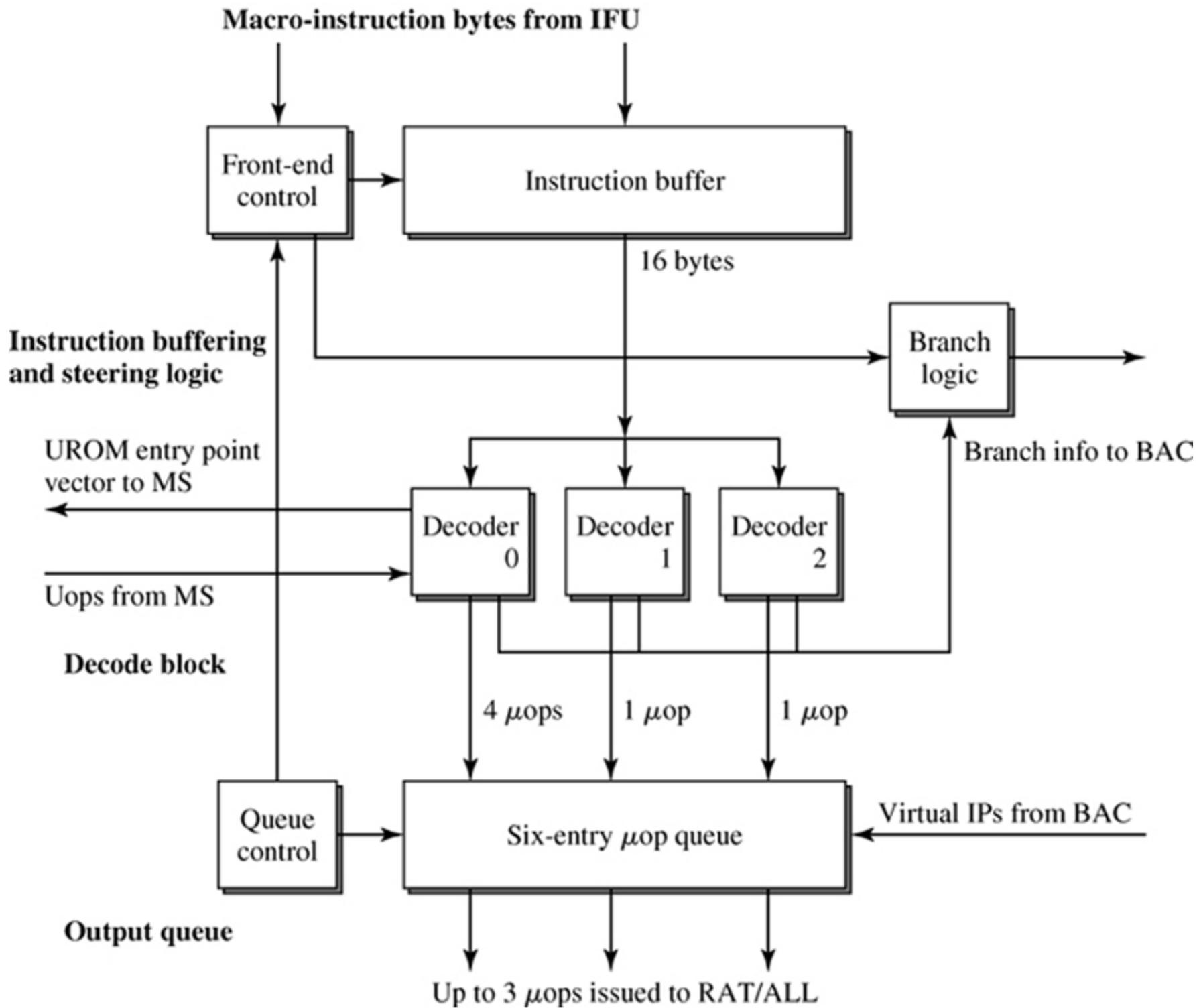


Figure 7.10: ID Block Diagram.

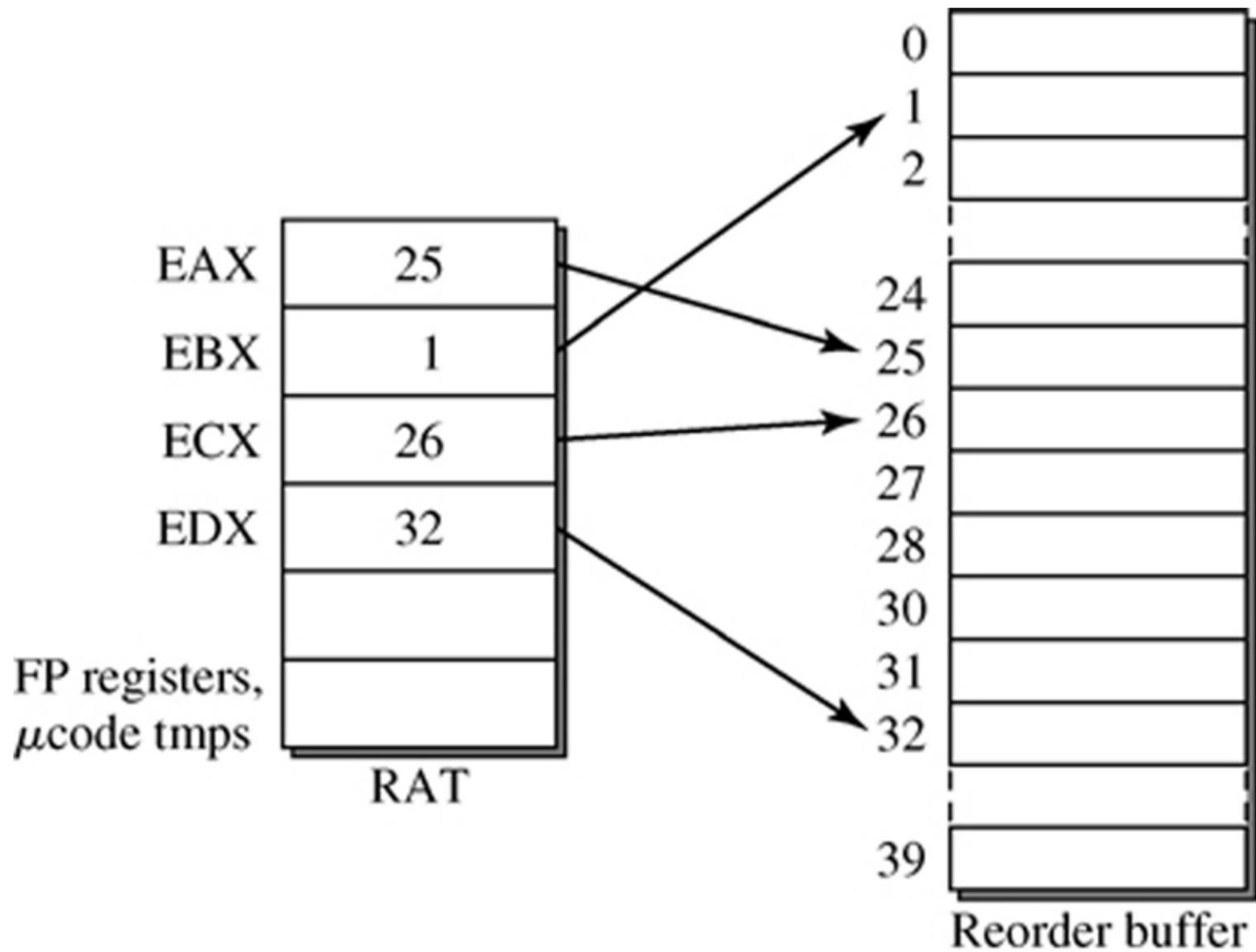


Figure 7.11: Basic RAT Register Renaming.

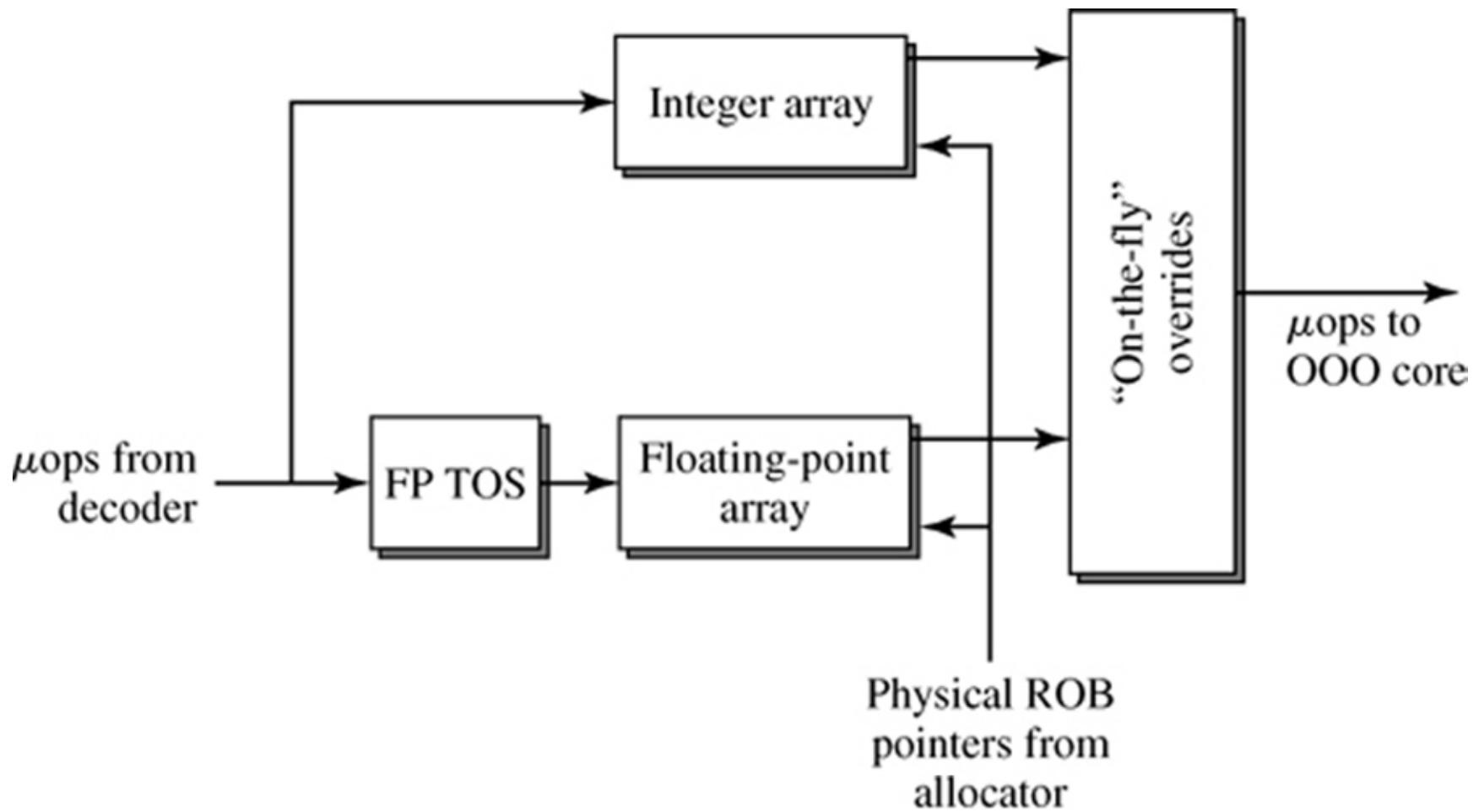


Figure 7.12: RAT Block Diagram.

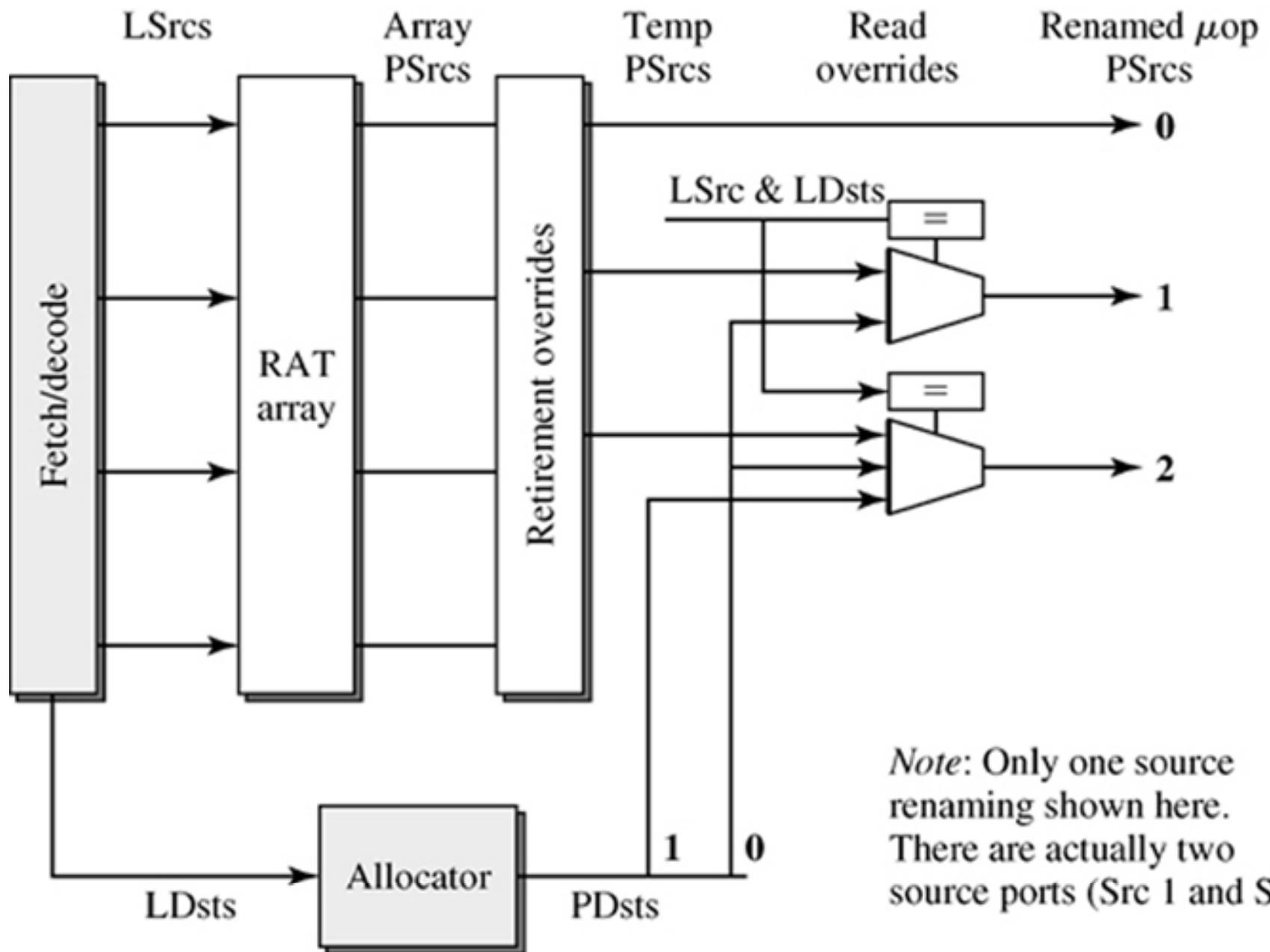


Figure 7.13: RAT new PDst Overrides.

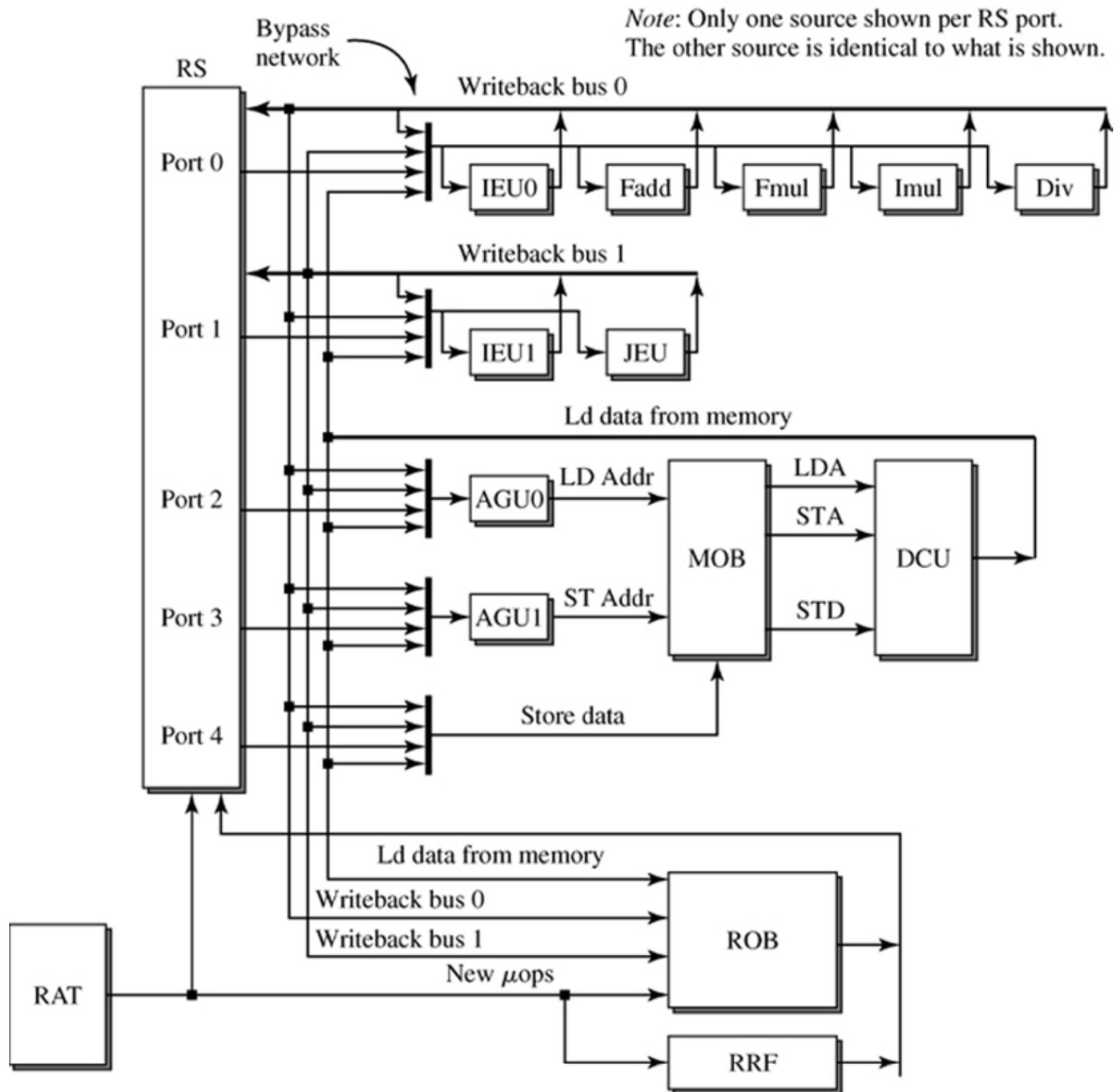


Figure 7.14:  
Execution Unit  
Data Paths.