Table 8.2
Out-of-order organization

Processor	Reservation Station Structure (Number of Entries)	Operand Copies	Entries in Reorder Buffer	Result Copies
Alpha 21264	Queues (15, 20)	No	20 × 4 insts. each	No
HP PA 8000	Queues (28, 28)	No	Combined w/RS	No
AMD K5	Decentralized (1, 2, 2, 2, 2, 2)	Yes	16	Yes
AMD K7	Schedulers (6 × 3, 12 × 3)	Yes, no	24 × 3 macroOps each	Yes, no
Pentium Pro	Centralized (20)	Yes	40	Yes
Pentium 4	Queues and schedulers	No	128	No
MIPS R10000	Queues (16, 16, 16)	No	32 (active list)	No
PPC 604	Decentralized (2, 2, 2, 2, 2, 2)	Yes	16	No
PPC 750	Decentralized (1, 1, 1, 1, 2, 2)	Yes	6	No
PPC 620	Decentralized (2, 2, 2, 2, 3, 4)	Yes	16	No
POWER3	Queues (3, 4, 6, 6, 8)	No	32	No
POWER4	Queues (10, 10, 10, 12, 18, 18)	No	20 × 5 IOPs each	No
SPARC64	Decentralized (8, 8, 8, 12)	Yes	64 (A-ring)	No

Table 8.2: Out-of-order execution.