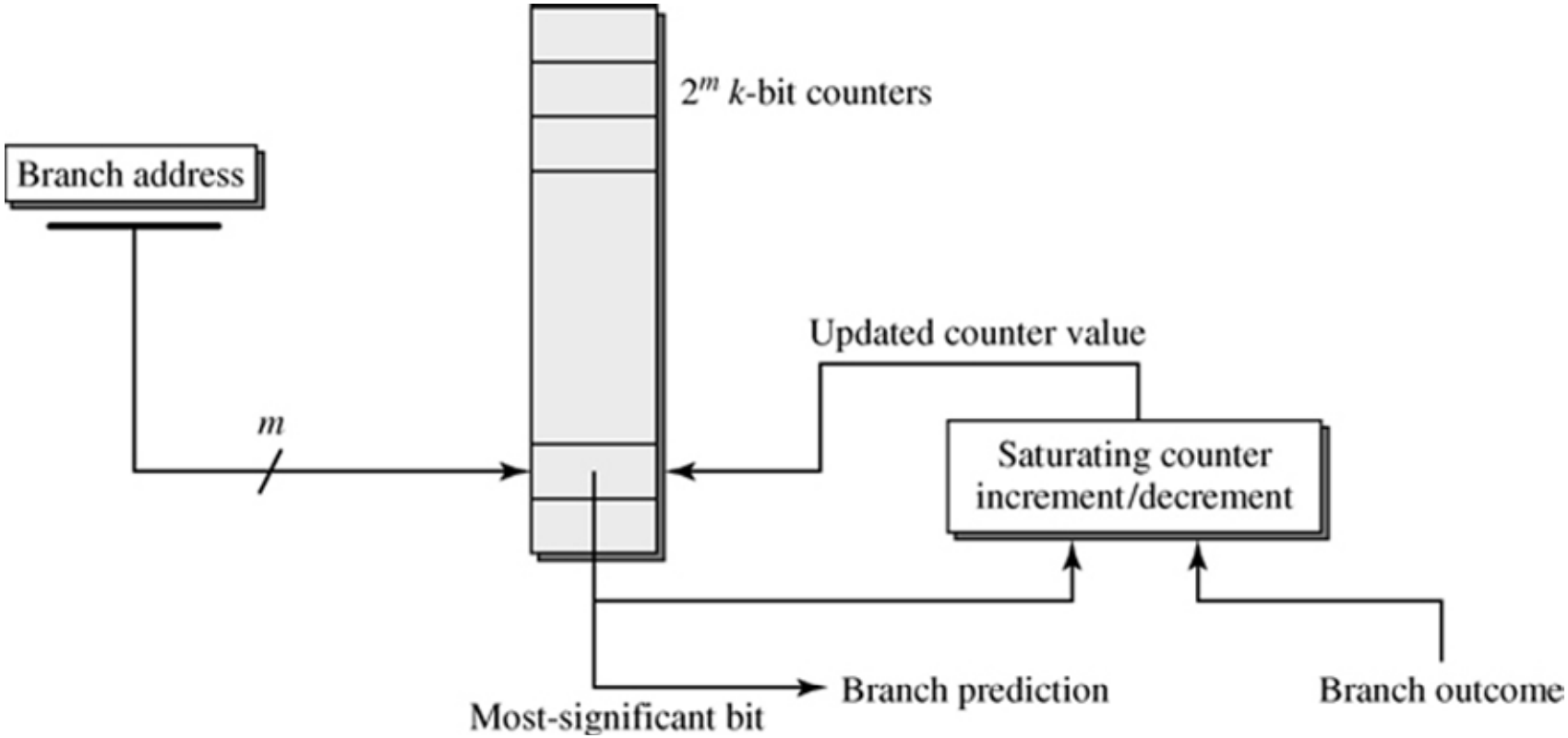

Figure 9.1: Smith Predictor with a 2^m-entry Table of Saturating k-bit counters.

Branch	Branch Direction	$Smith_1$		$Smith_2$	
		State	Prediction	State	Prediction
A	1	1	1	11	1
B	1	1	1	11	1
C	0	1	1 (misprediction)	11	1 (misprediction)
D	1	0	0 (misprediction)	10	1
E	1	1	1	11	1
F	1	1	1	11	1

Figure 9.2

A Comparison of a $Smith_1$ and a $Smith_2$ Predictor on a Sequence of Branches with a Single Anomalous Decision.

Figure 9.2: A Comparison of a $Smith_1$ and a $Smith_2$ Predictor on a Squence of Branches iwth a Single Anomalous Decision.

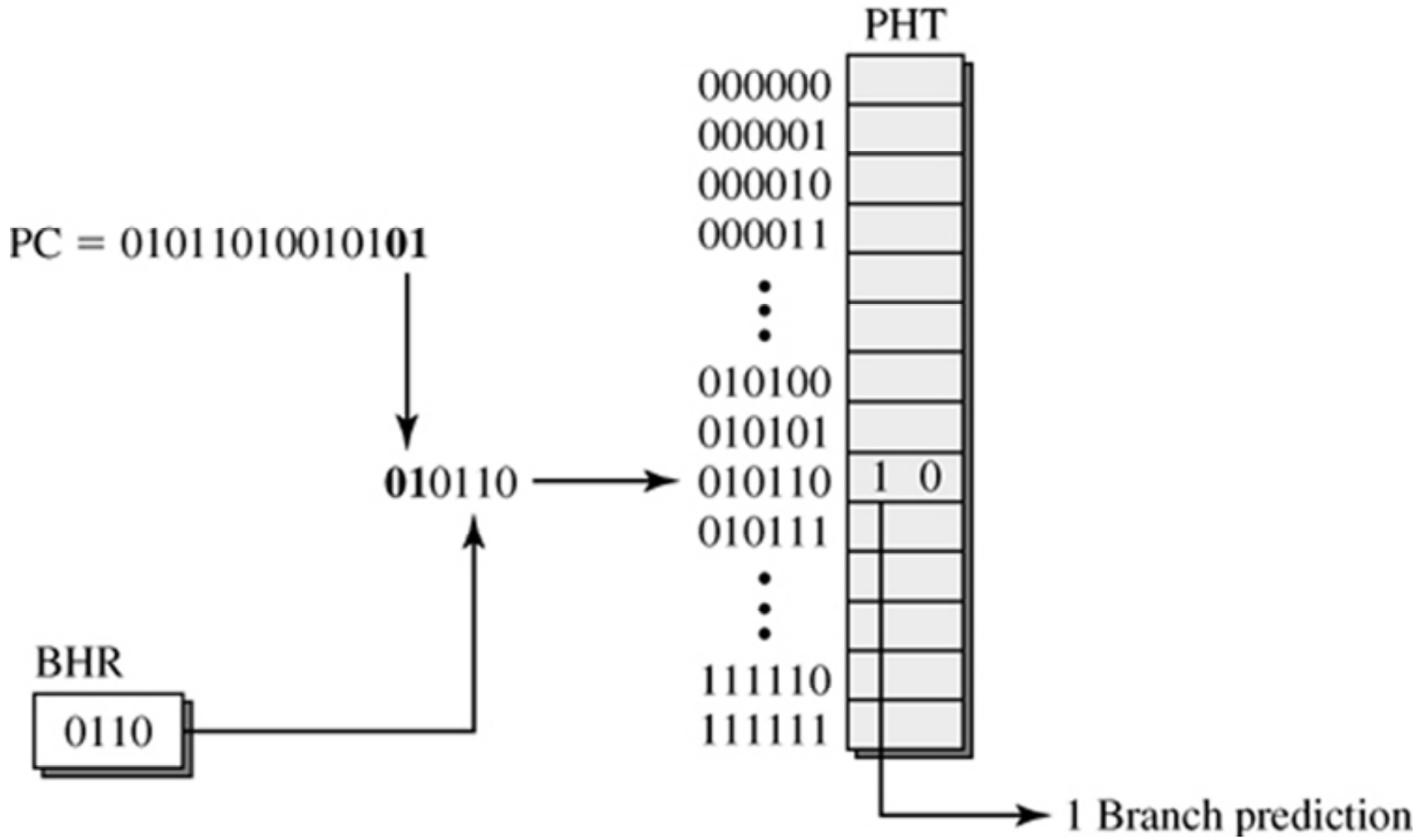

Figure 9.3: A Global-History Two-Level Predictor with a 4-bit Branch History Register

```
x = 0;
if (someCondition) {          /* branch A */
     x = 3;
}
if (someOtherCondition) {     /* branch B */
     y += 19;
}
if (x <= 0) {                 /* branch C */
     doSomething( );
}
```

Figure 9.4

A Sample Code Segment with Correlated Branches.

Figure 9.4: A Sample Code Segment with Correlated Branches

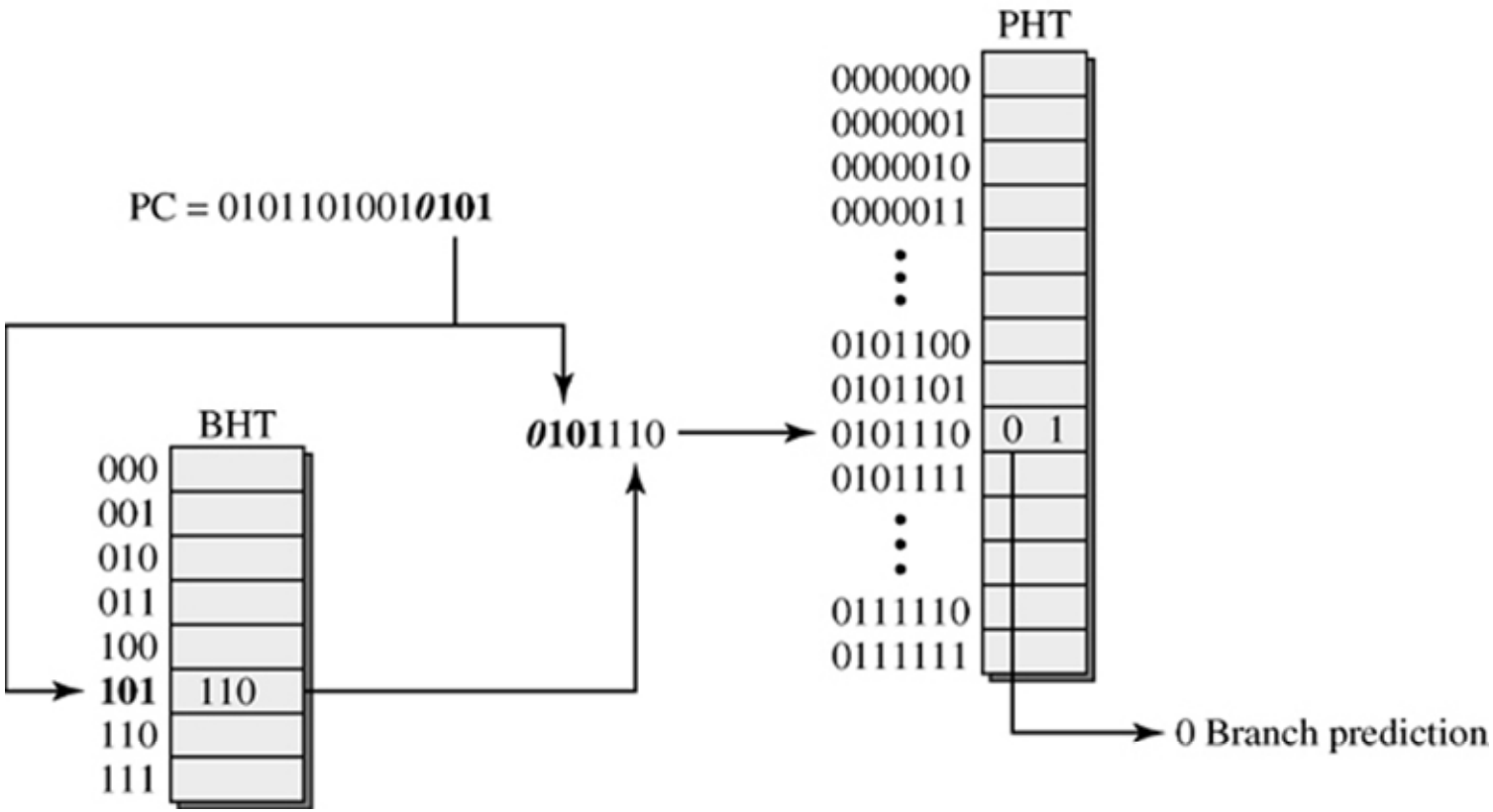

Figure 9.5: A Local-History Two-Level Predictor with an Eight-Entry BHT and a 3-bit History Length

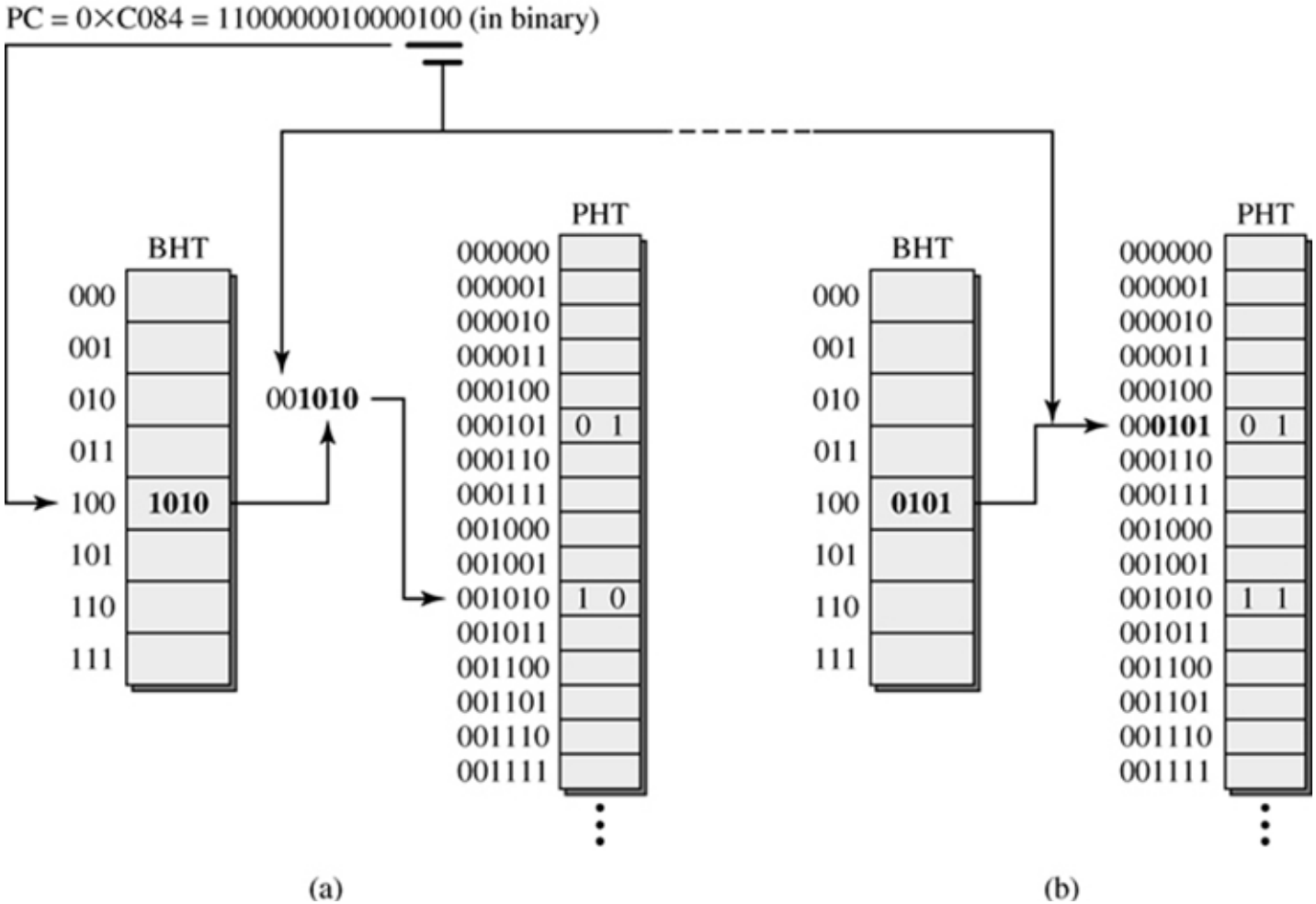

Figure 9.6: An Example Lookup on a Two-Level Branch Predictor: (a) Making the Prediction, and (b) After the Predictor Update

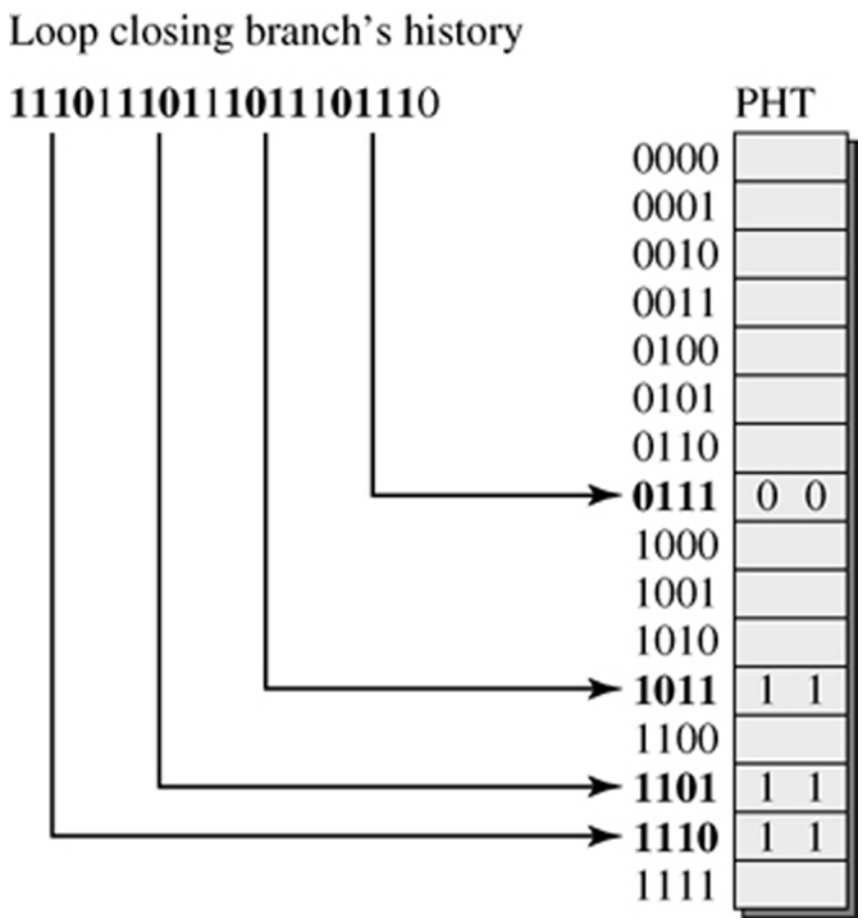

Figure 9.7: Local History Predictor Example

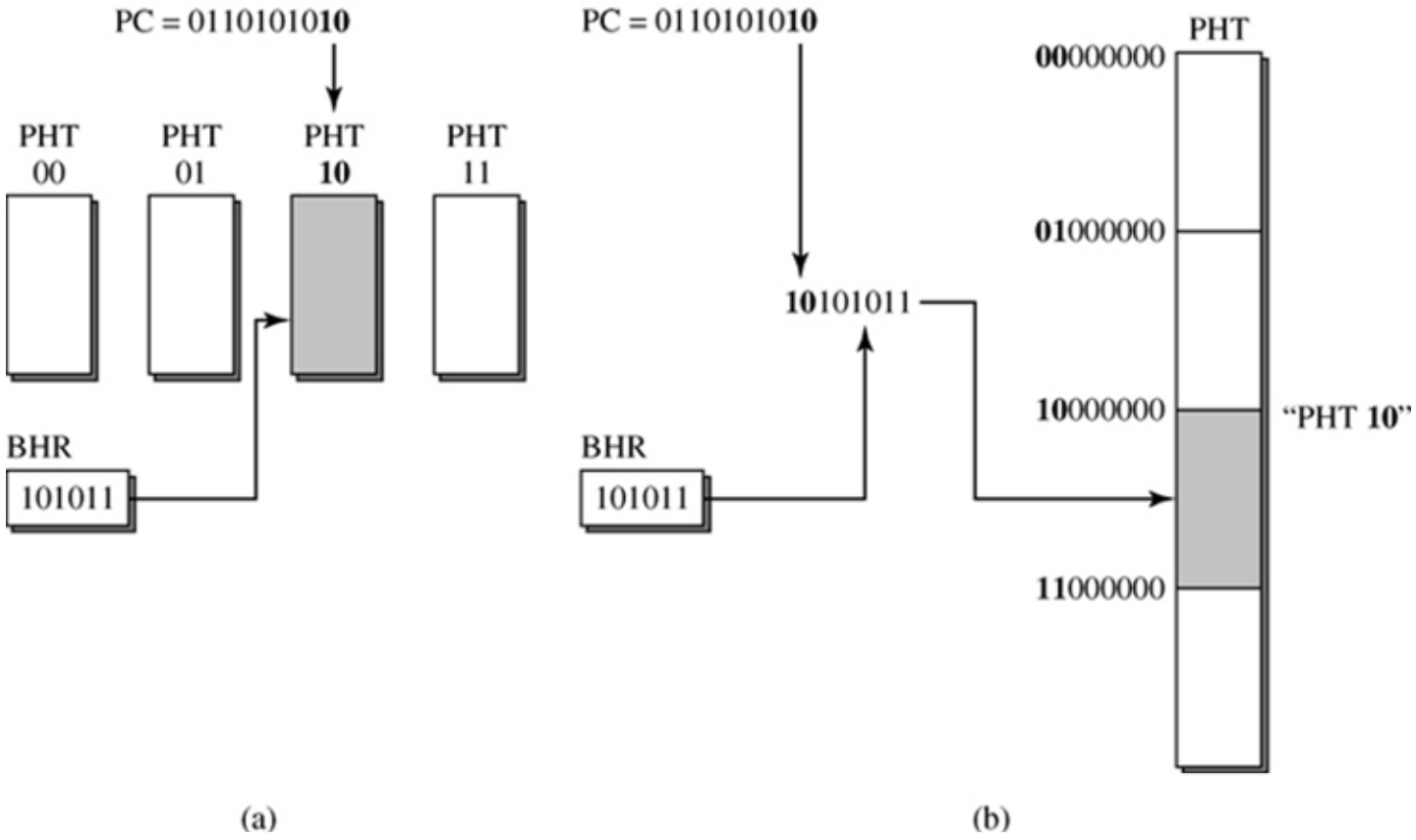

Figure 9.8: Alternative Views of the PHT Organization: (a) A Collection of PHTs, and (b) A Single Monolithic PHT.

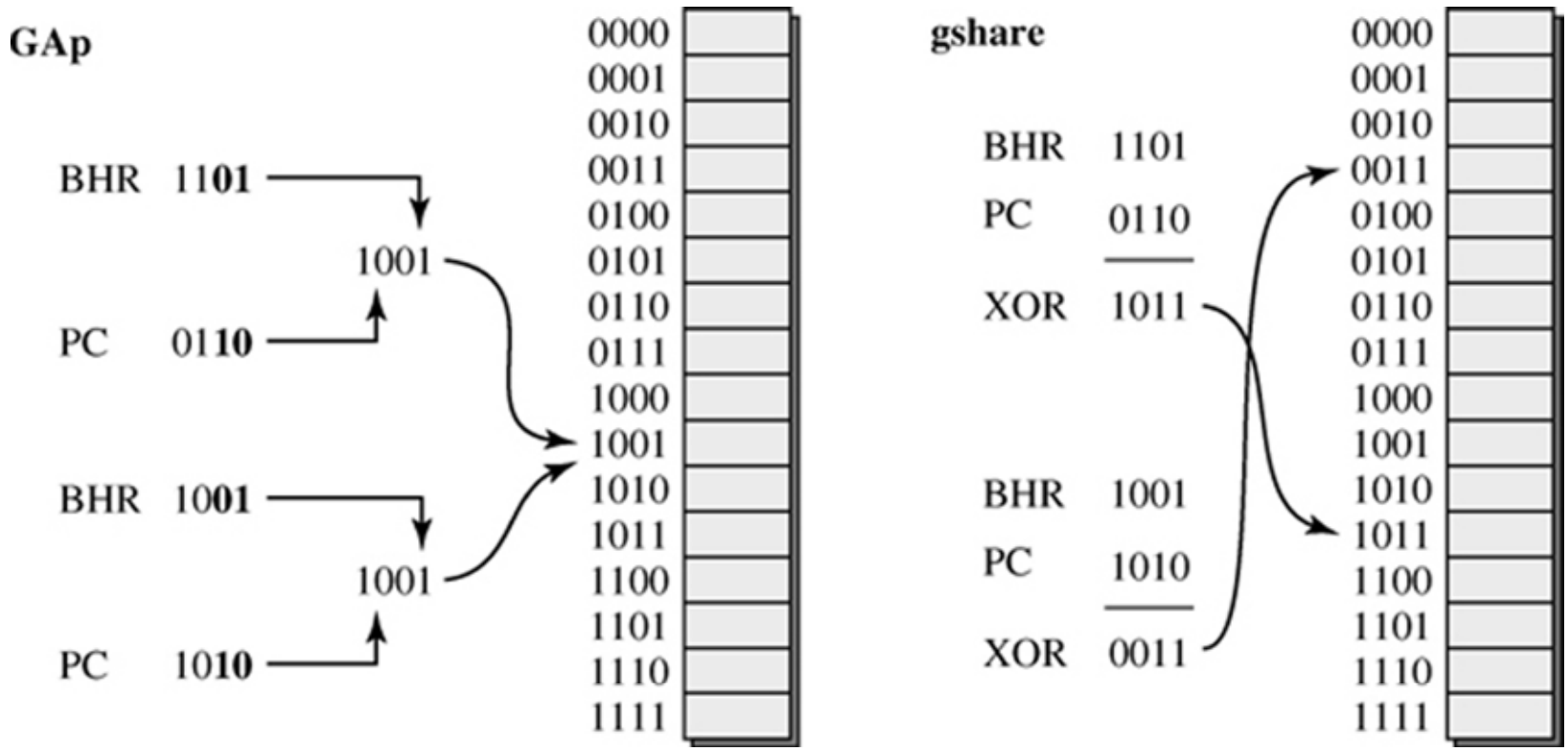

Figure 9.9: Indexing Example with a Global-History Two-Level Predictor and the gshare Predictor

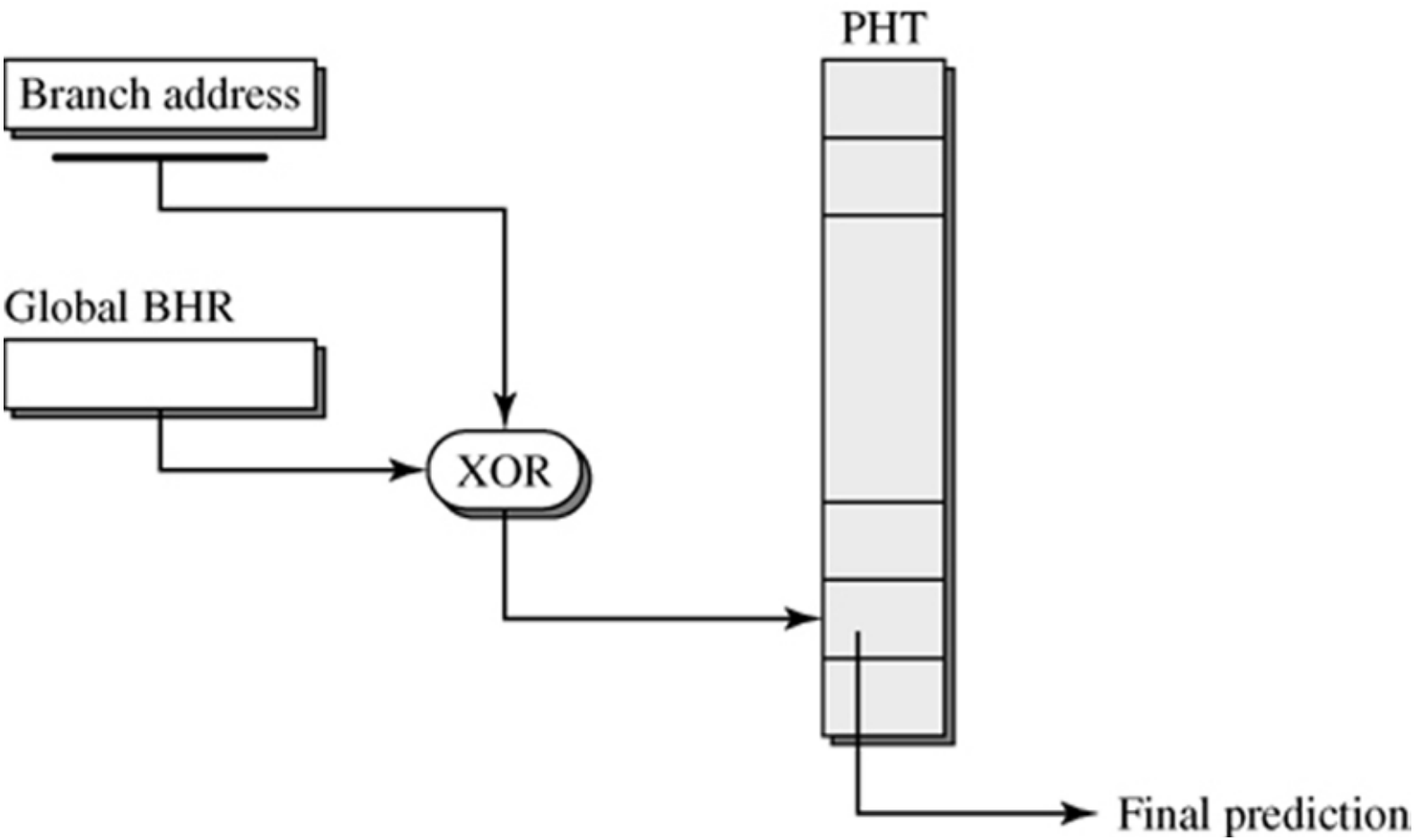

Figure 9.10: The gshare Predictor.

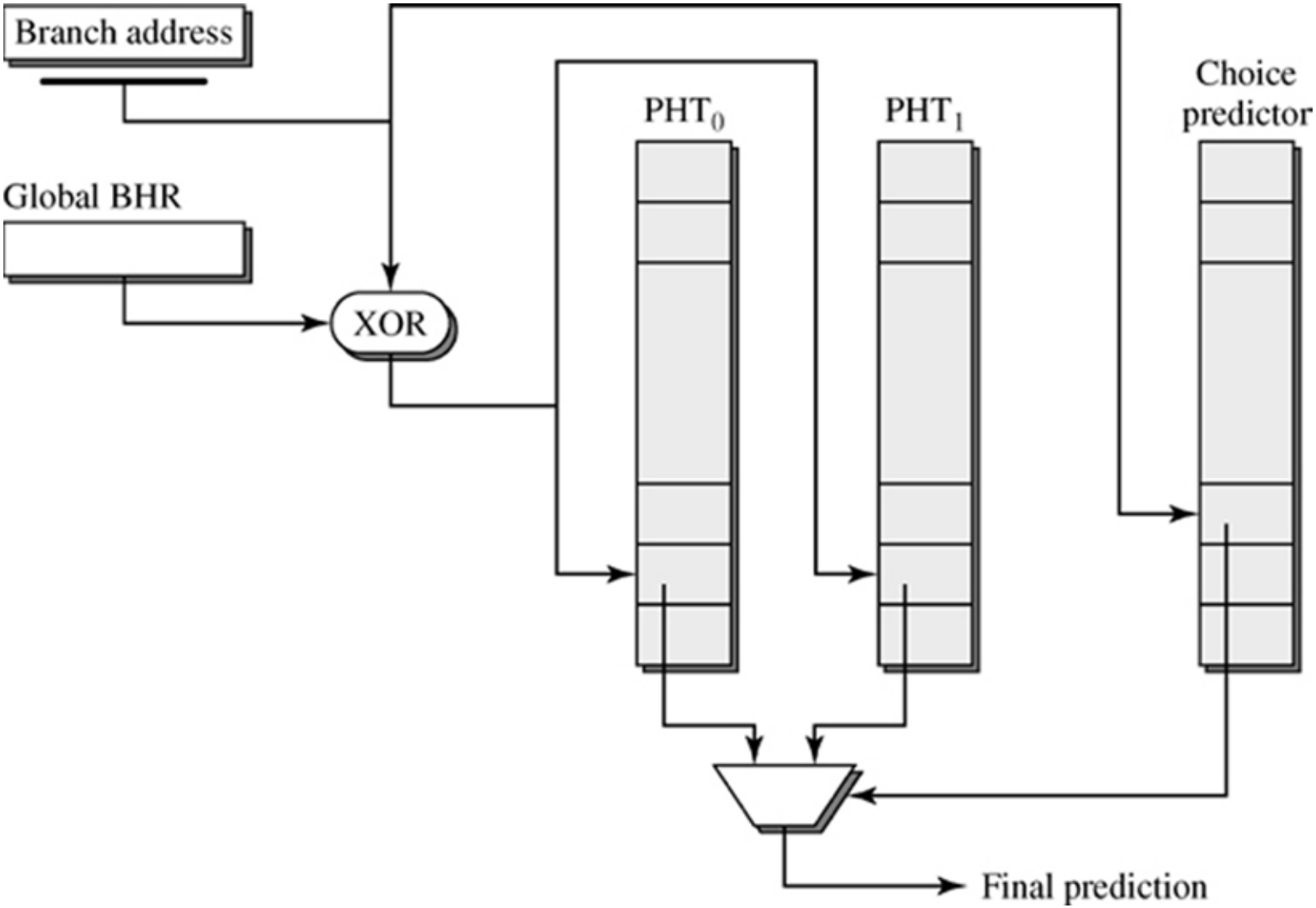

Figure 9.11: The Bi-Mode Predictor.

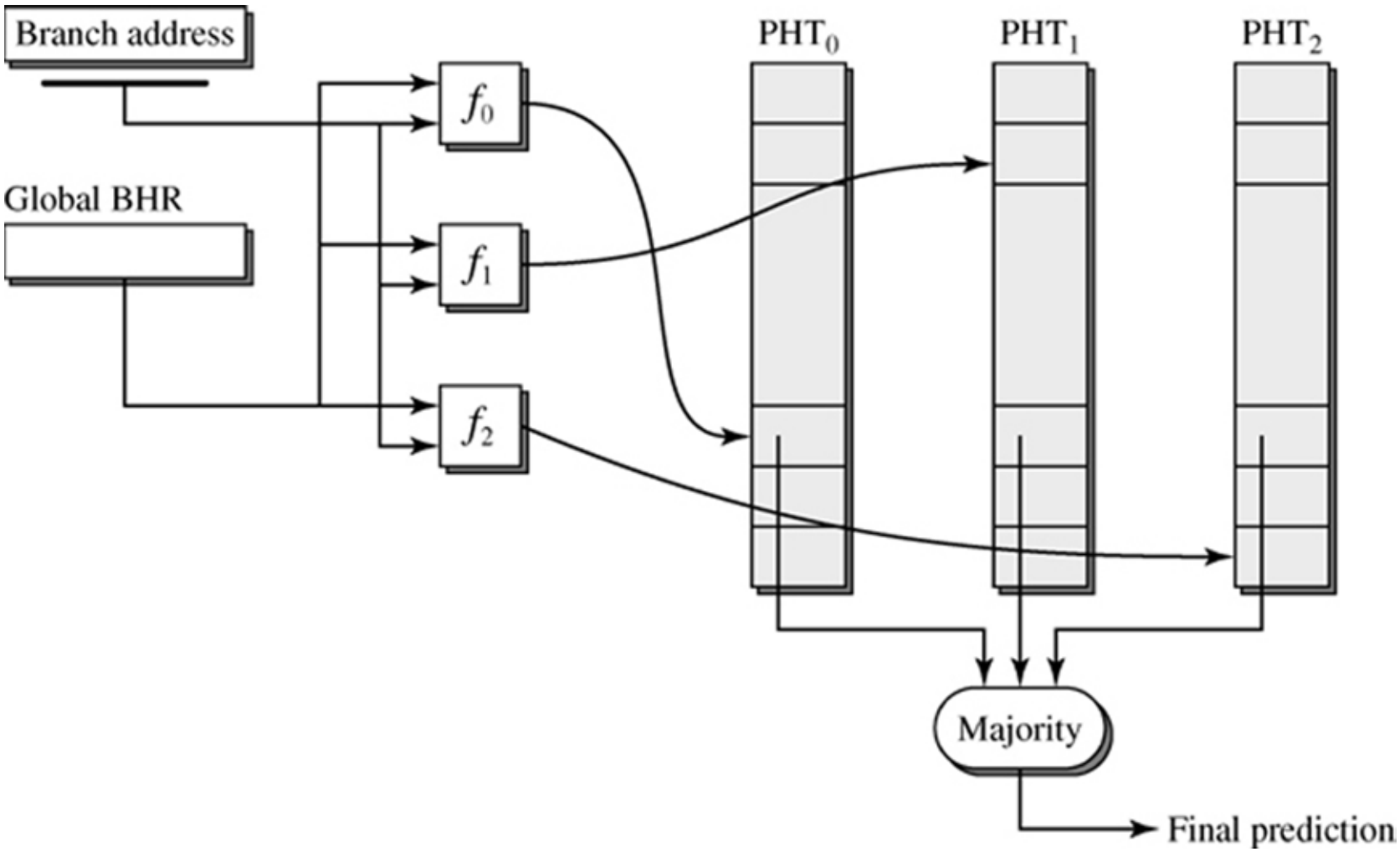

Figure 9.12: The gskewed Predictor.

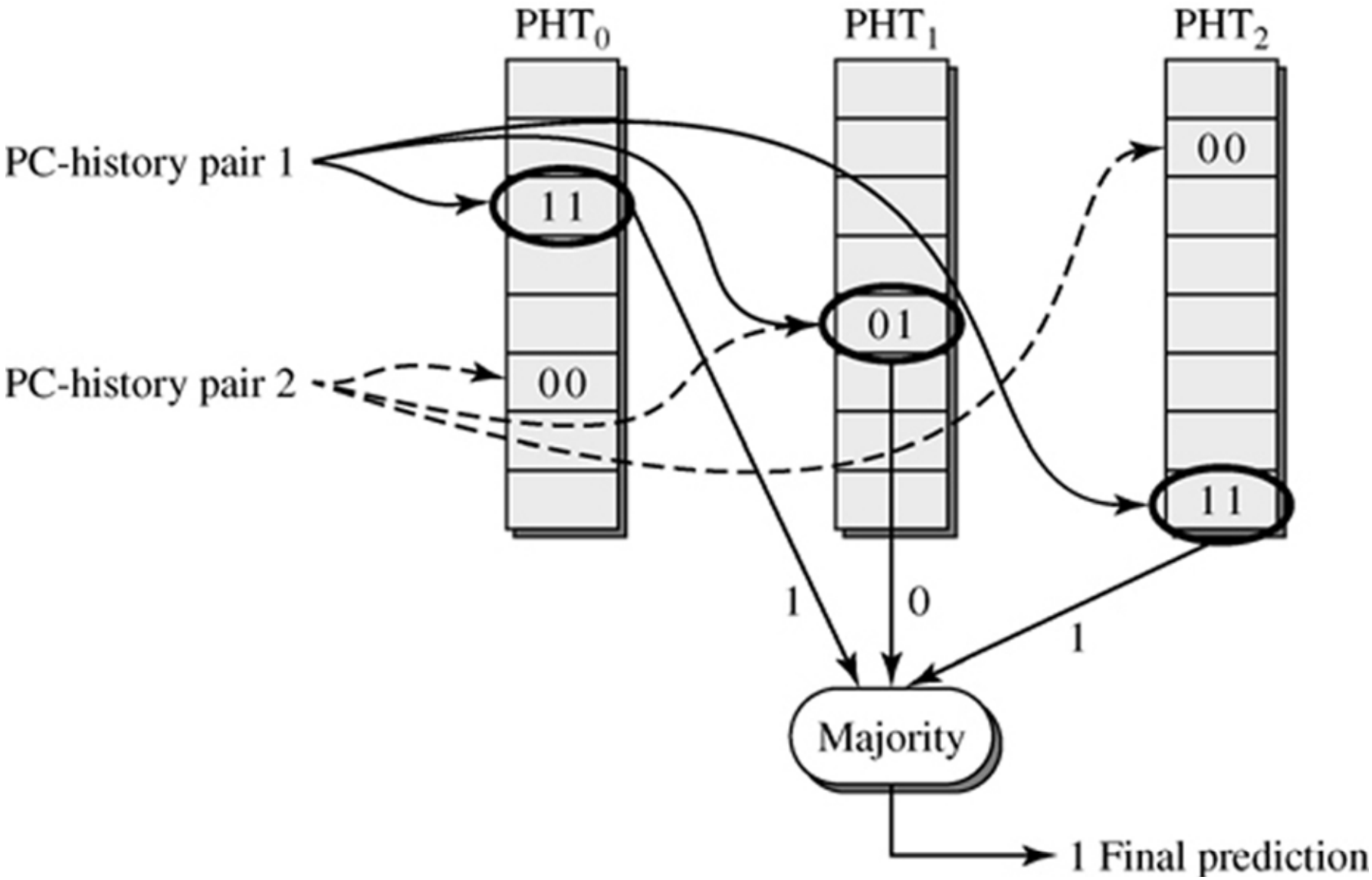

Figure 9.13: A gskewed Example Showing How the Majority Function Can Tolerate Interference in One of the PHT Banks.

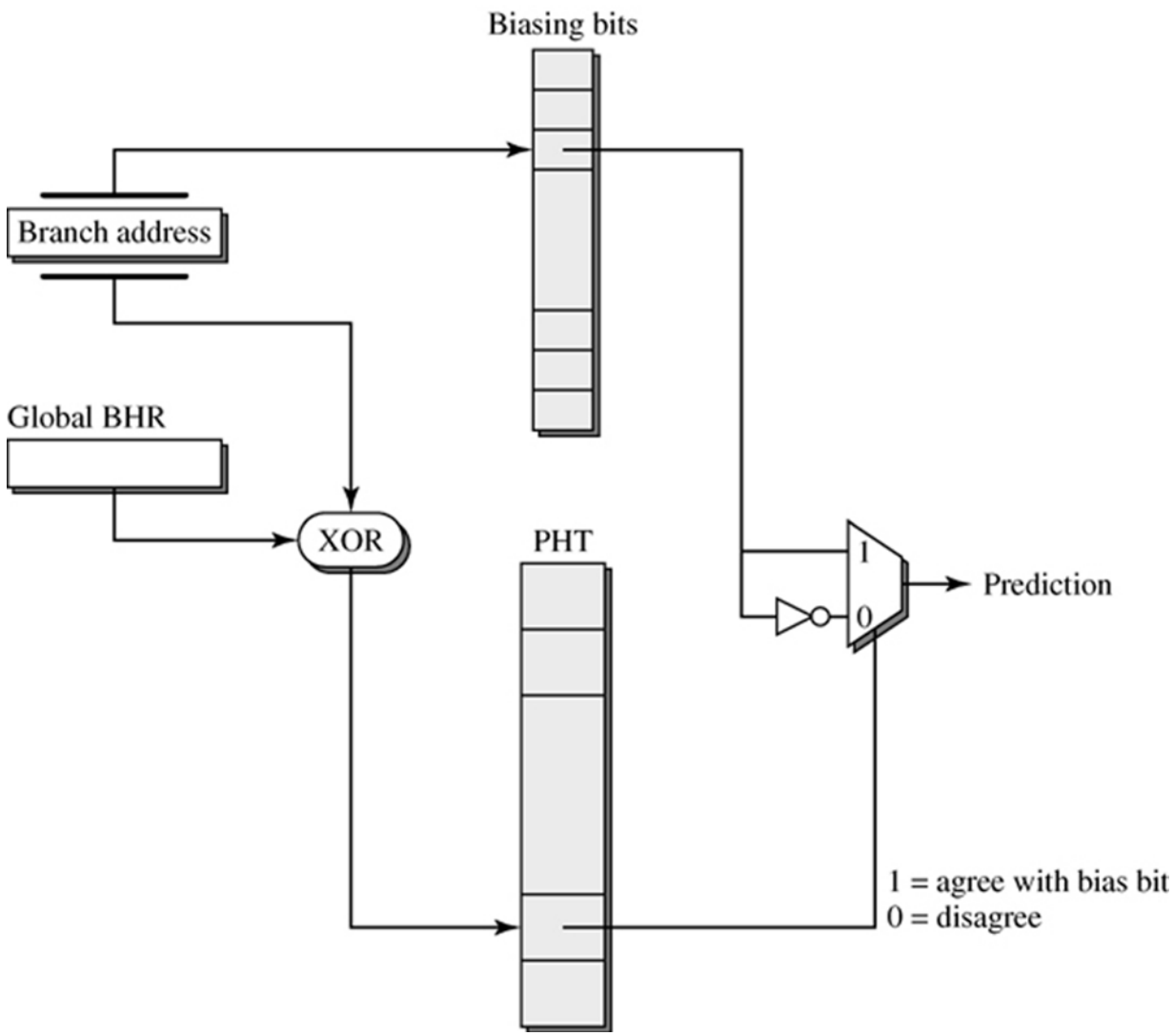

Figure 9.14: The Agree Predictor.

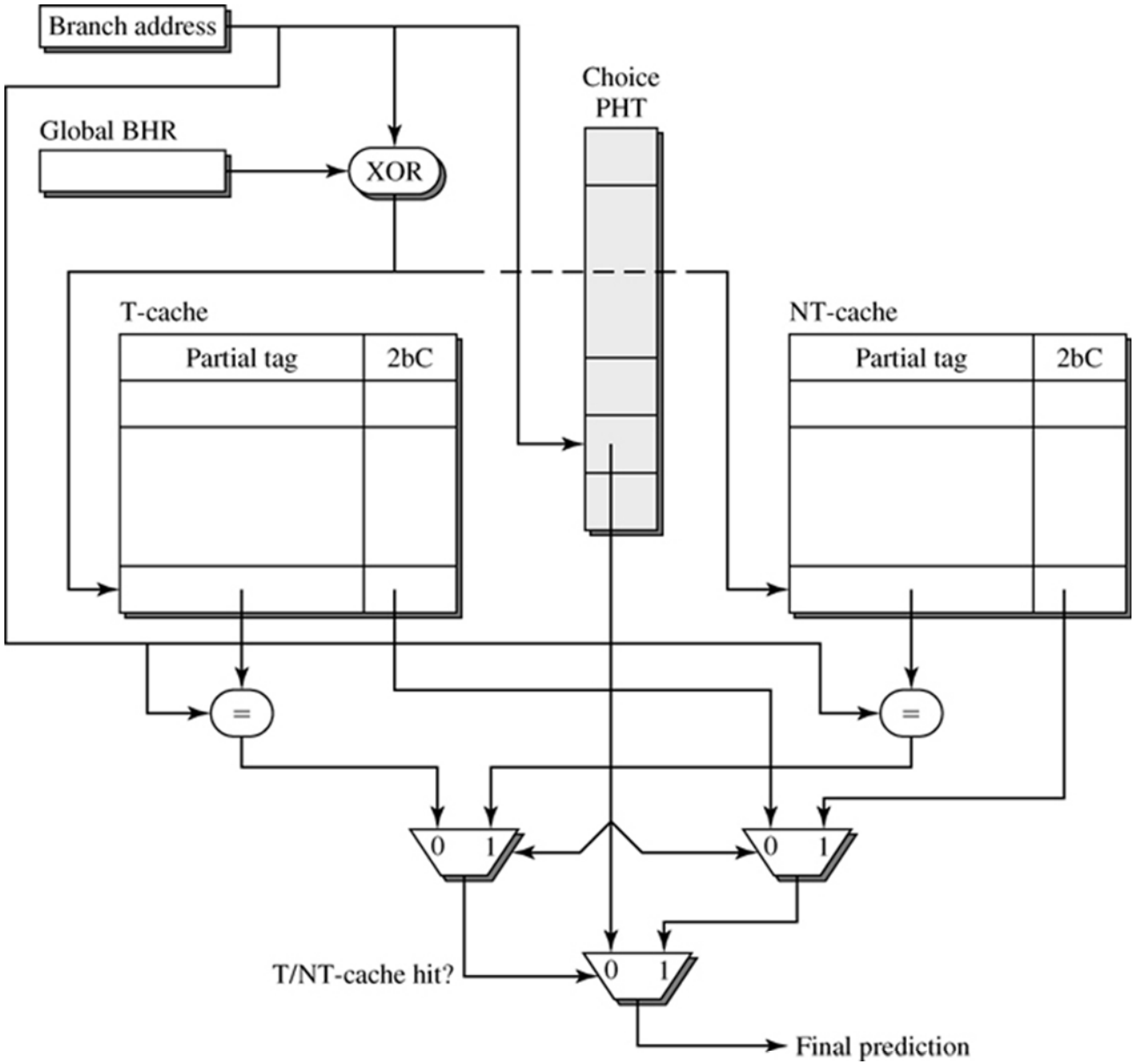

Figure 9.15: The YAGS Predictor.

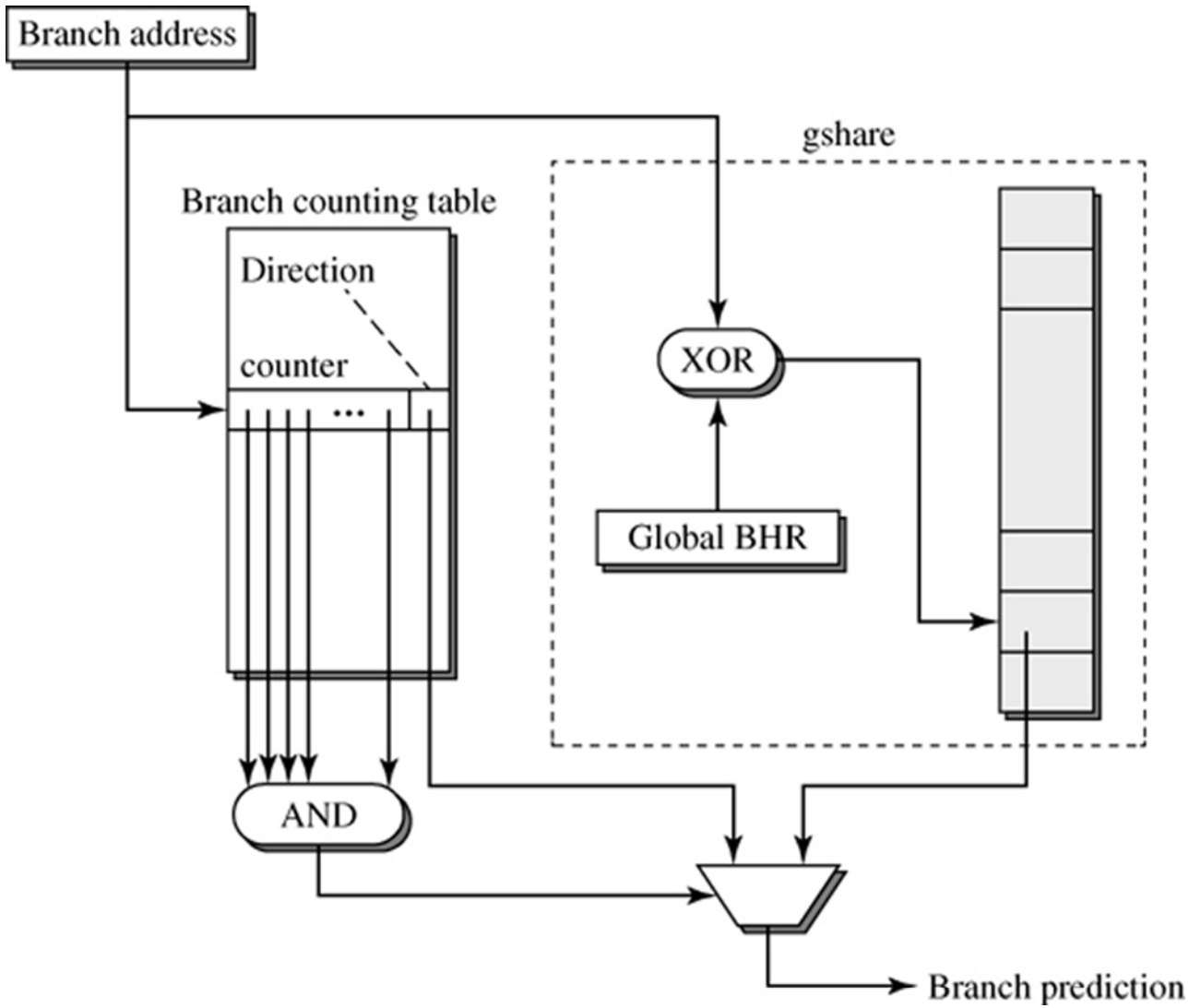

Figure 9.16: Branch Filtering Applied to a gshare Predictor.

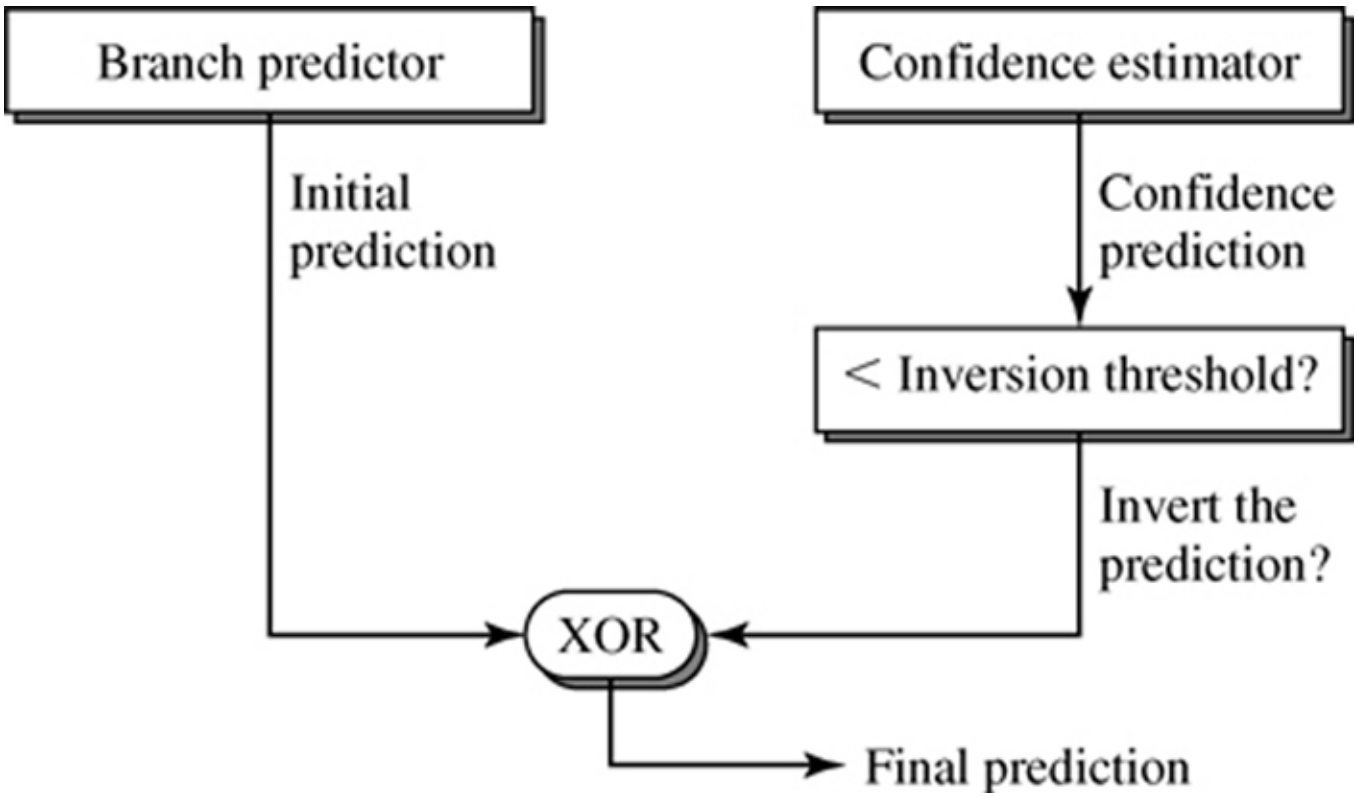

Figure 9.17: Selective Branch Inversion Applied to a Generic Branch Predictor.

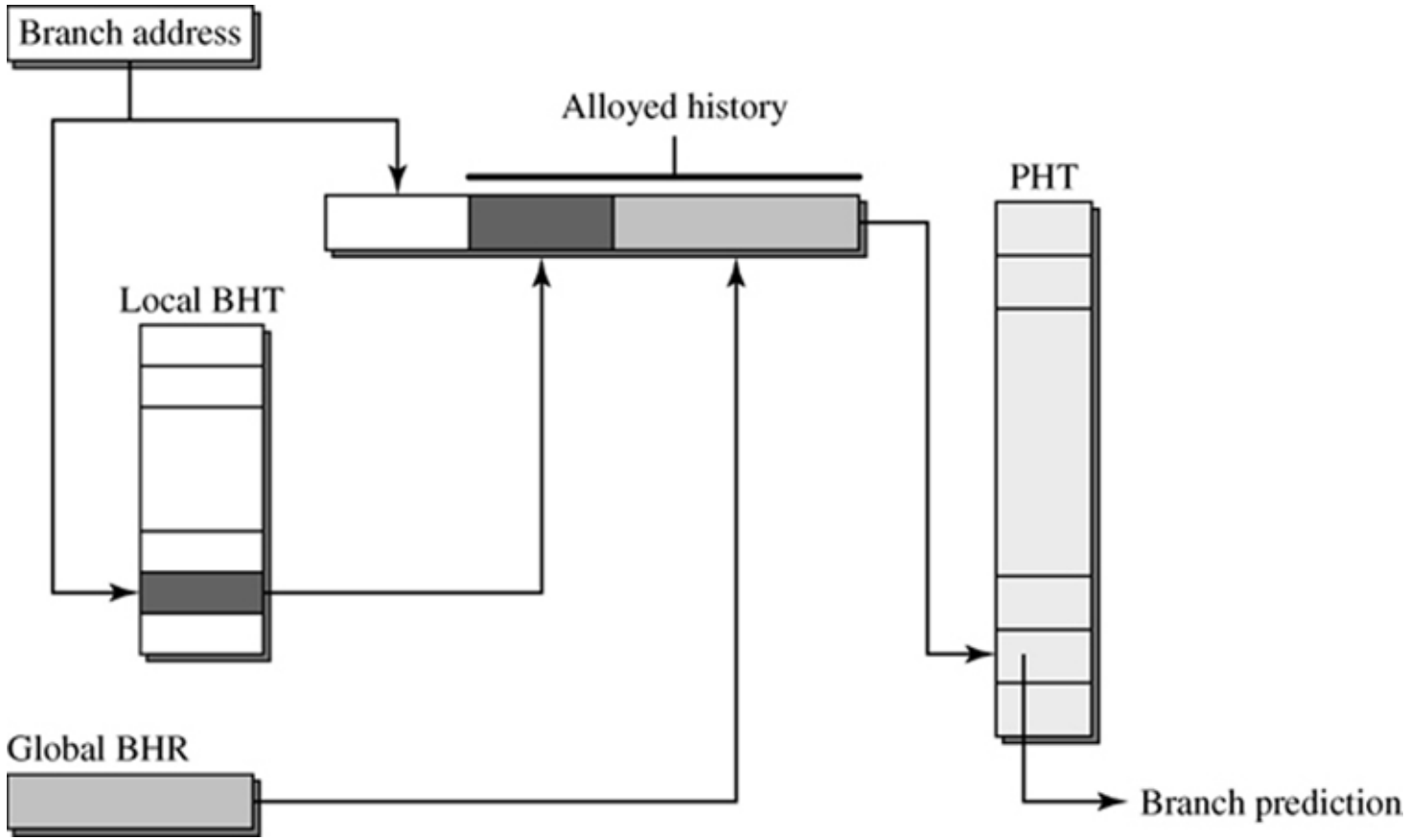

Figure 9.18: The Alloyed History Predictor.

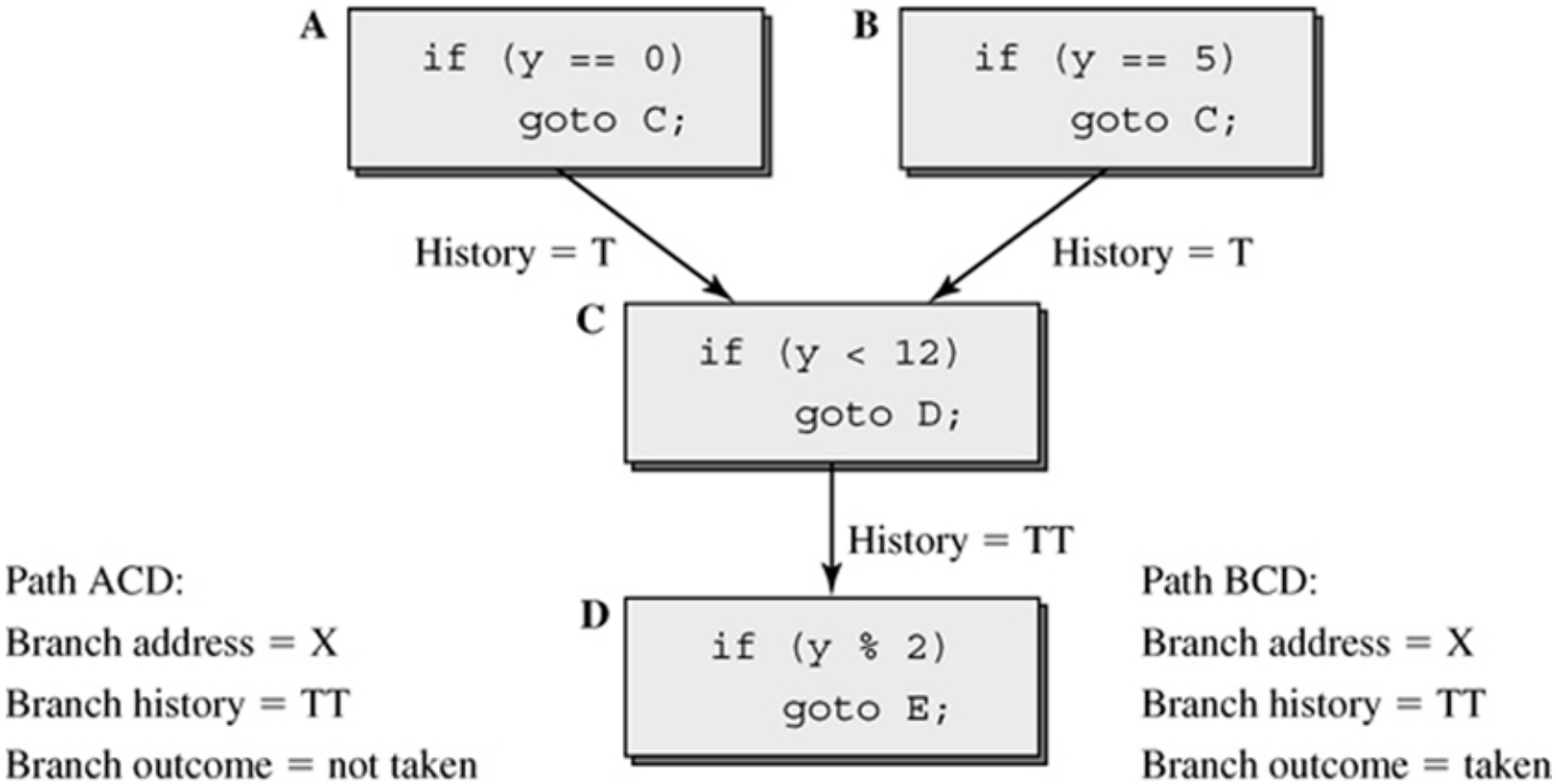

Figure 9.19: Path History Example.

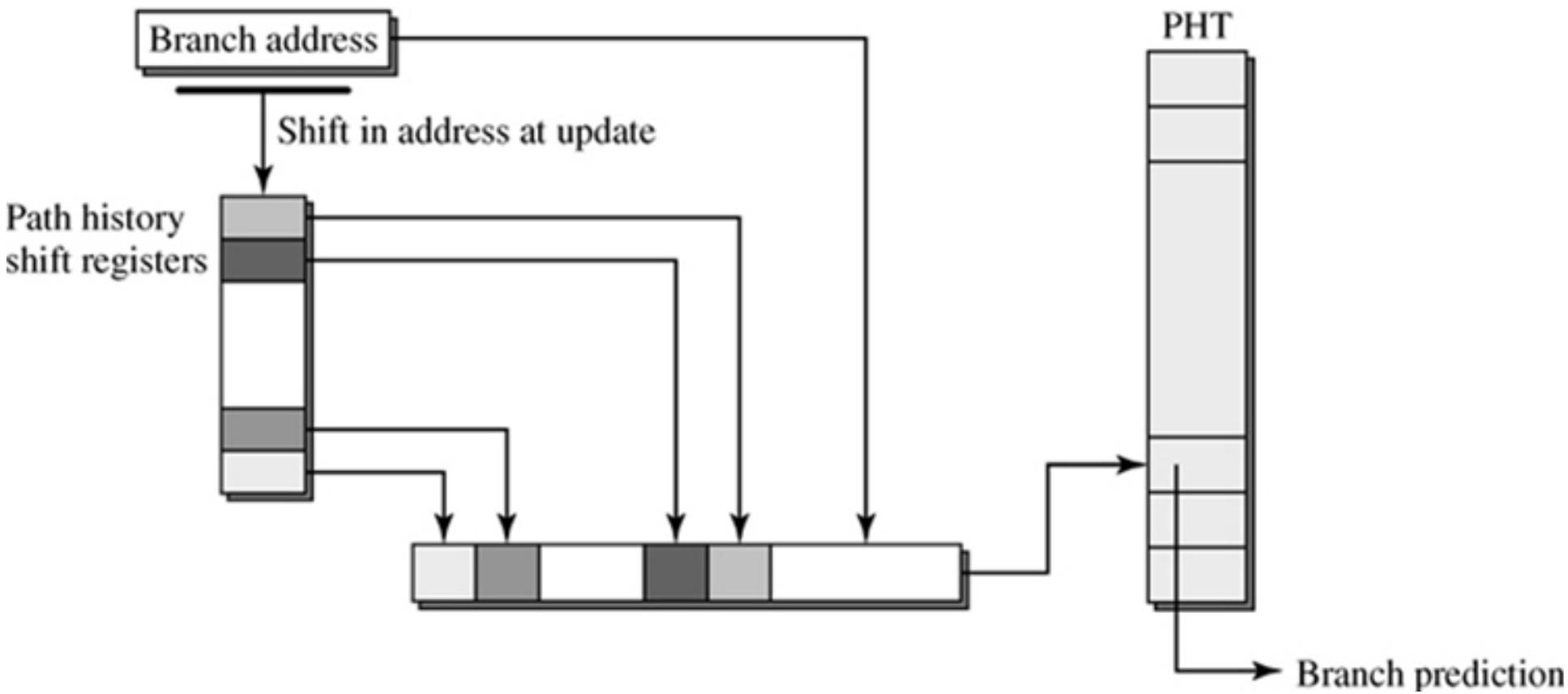

Figure 9.20: A Path History Predictor.

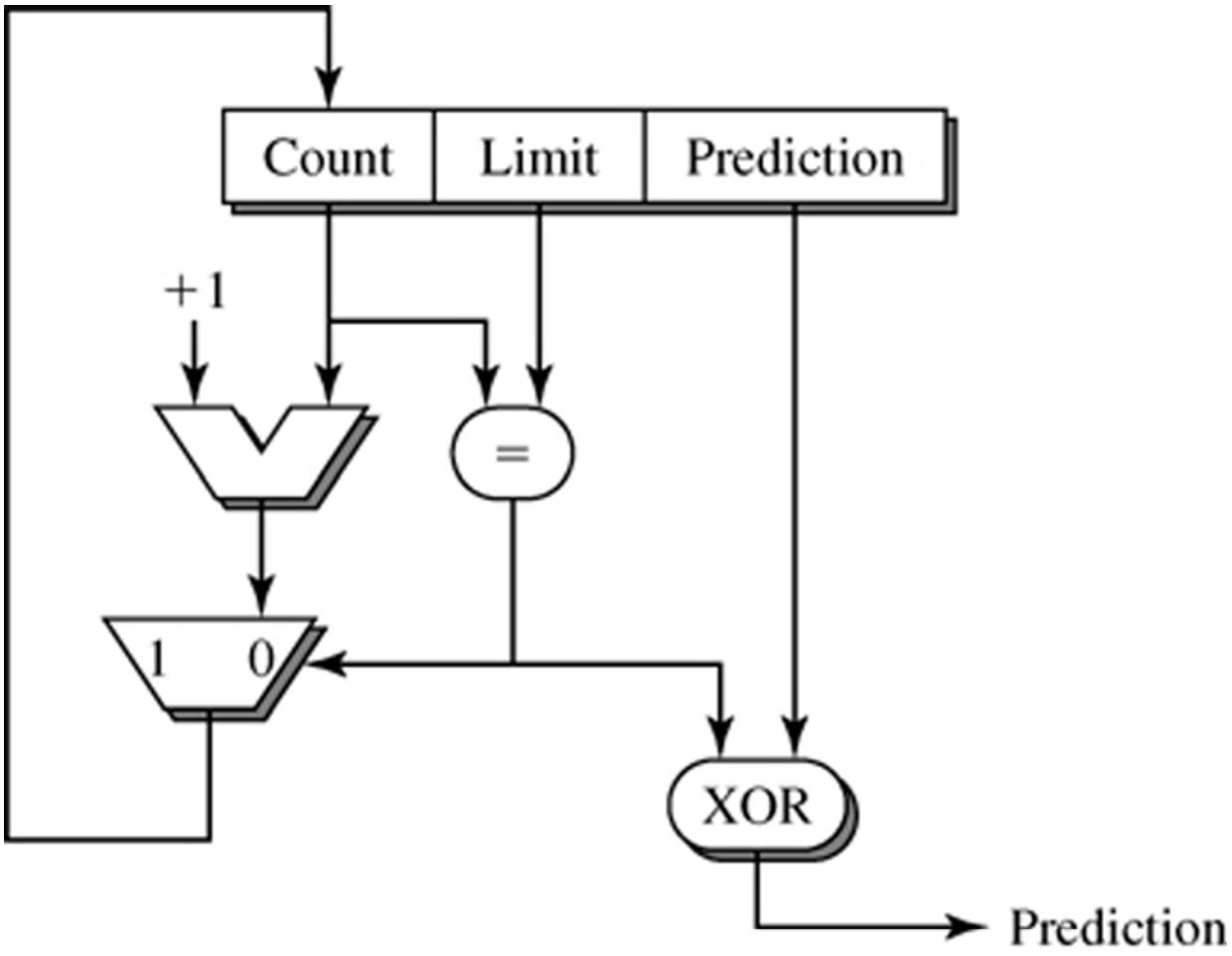

Figure 9.21: A Single Entry of the Loop Predictor Table Used in the Pentium-M Processor.

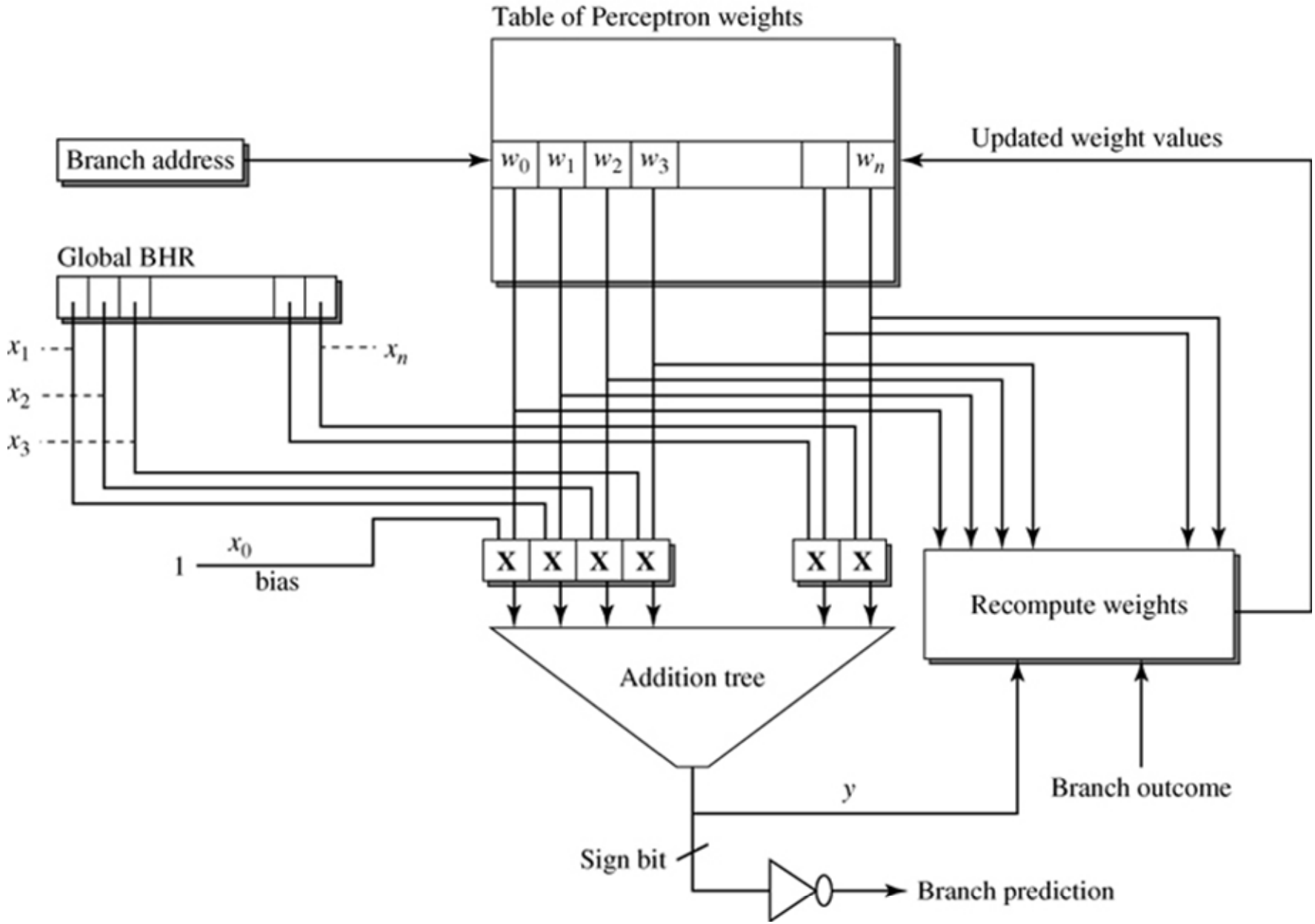

Figure 9.22: The Perceptron Predictor.

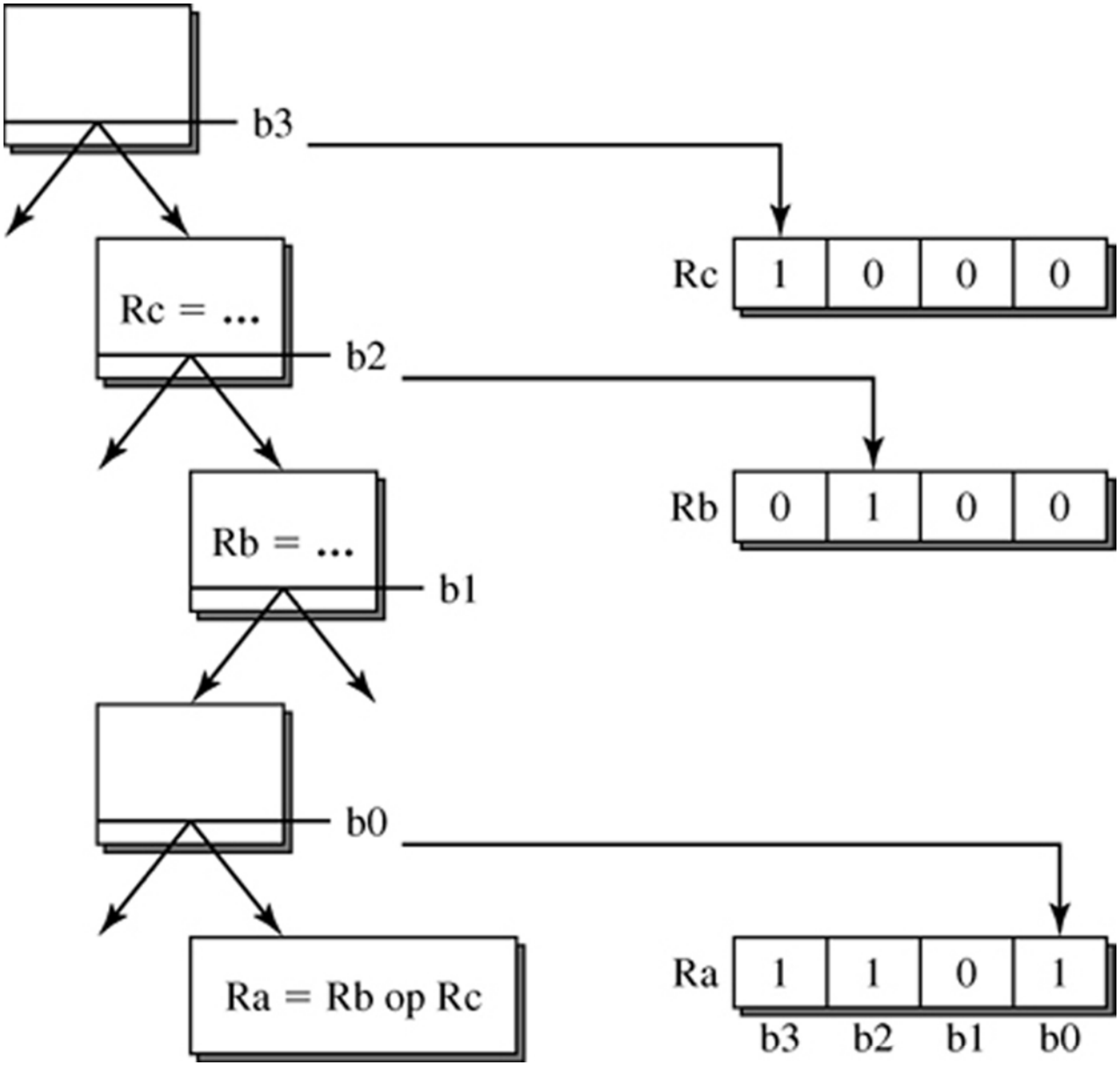

Figure 9.23: Affector Register File Update for a Register Writing Instruction.

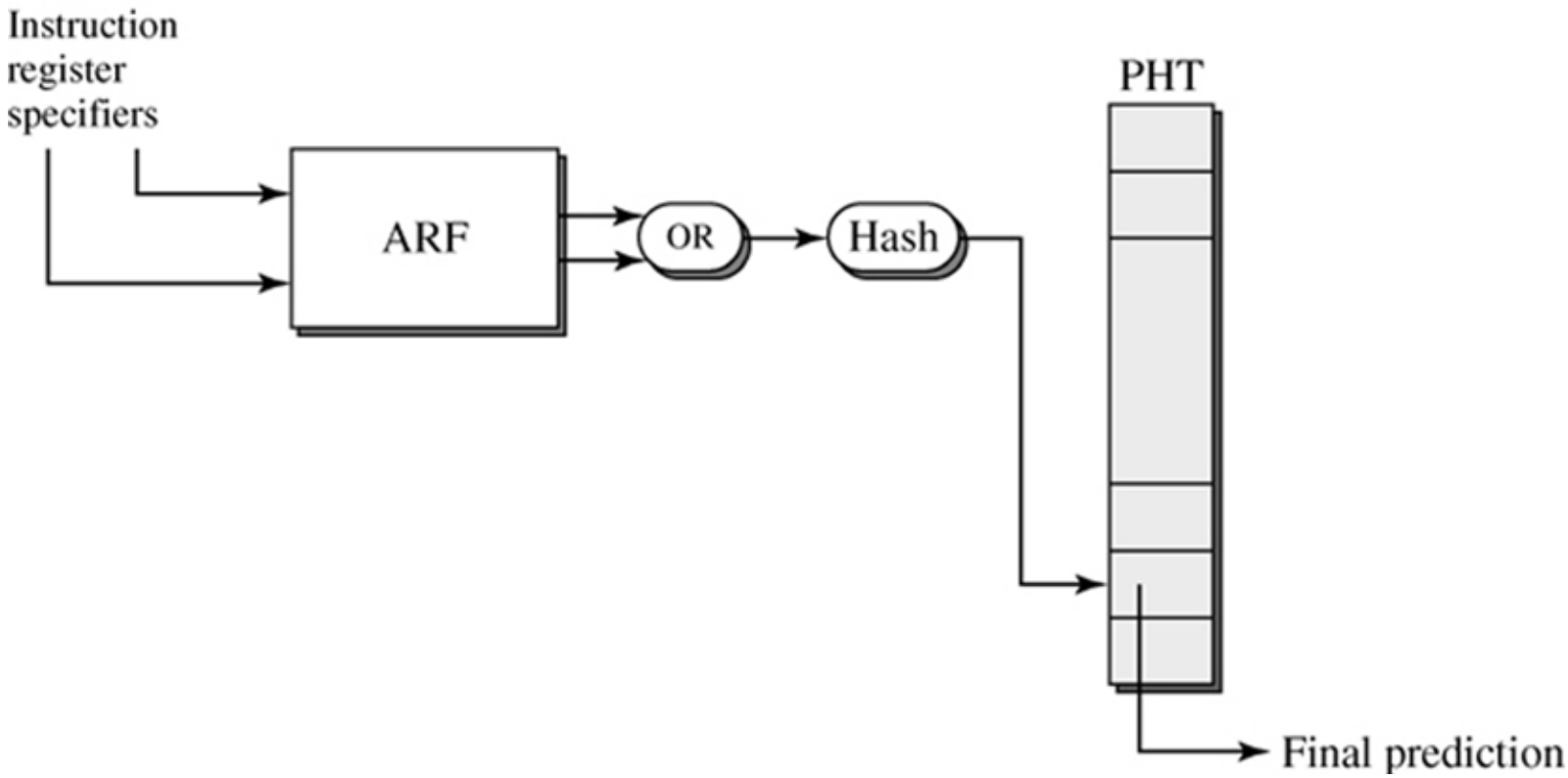

Figure 9.24: The Data Flow Branch Predictor.

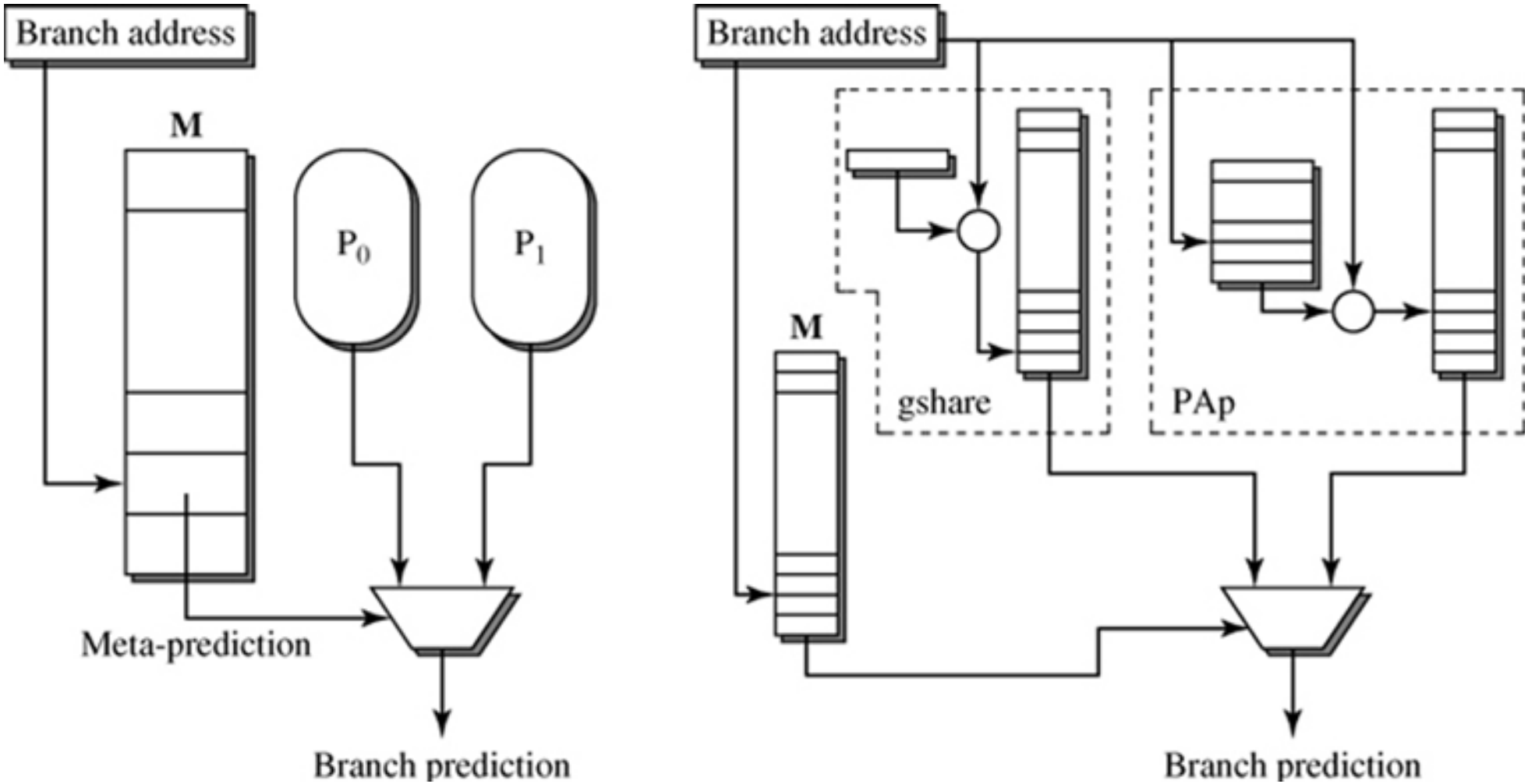

Figure 9.25: (a) The Tournament Selection Mechanism. (b) Tournament Hybrid with gshare and Pap.

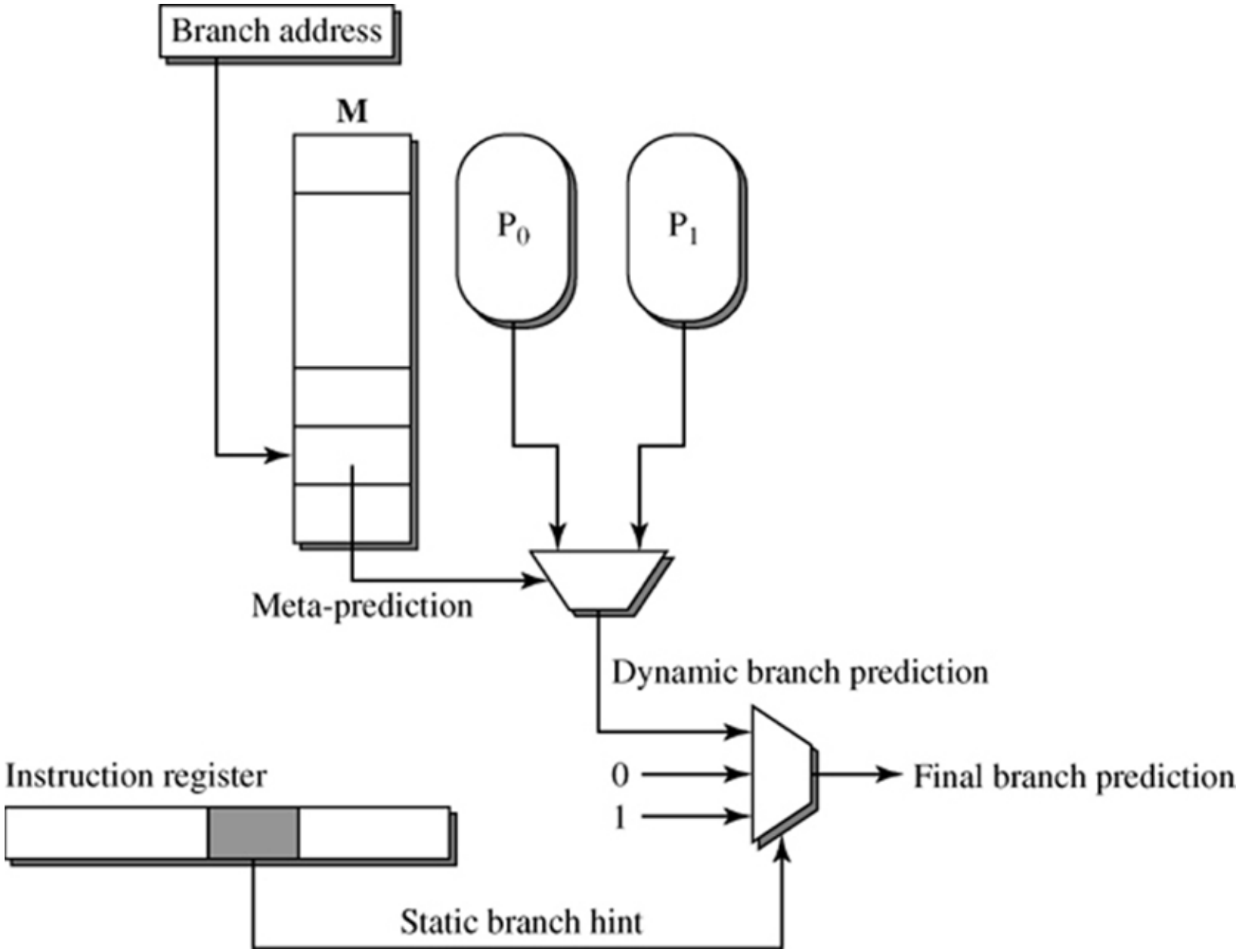

Figure 9.26: The Branch Classification Mechanism.

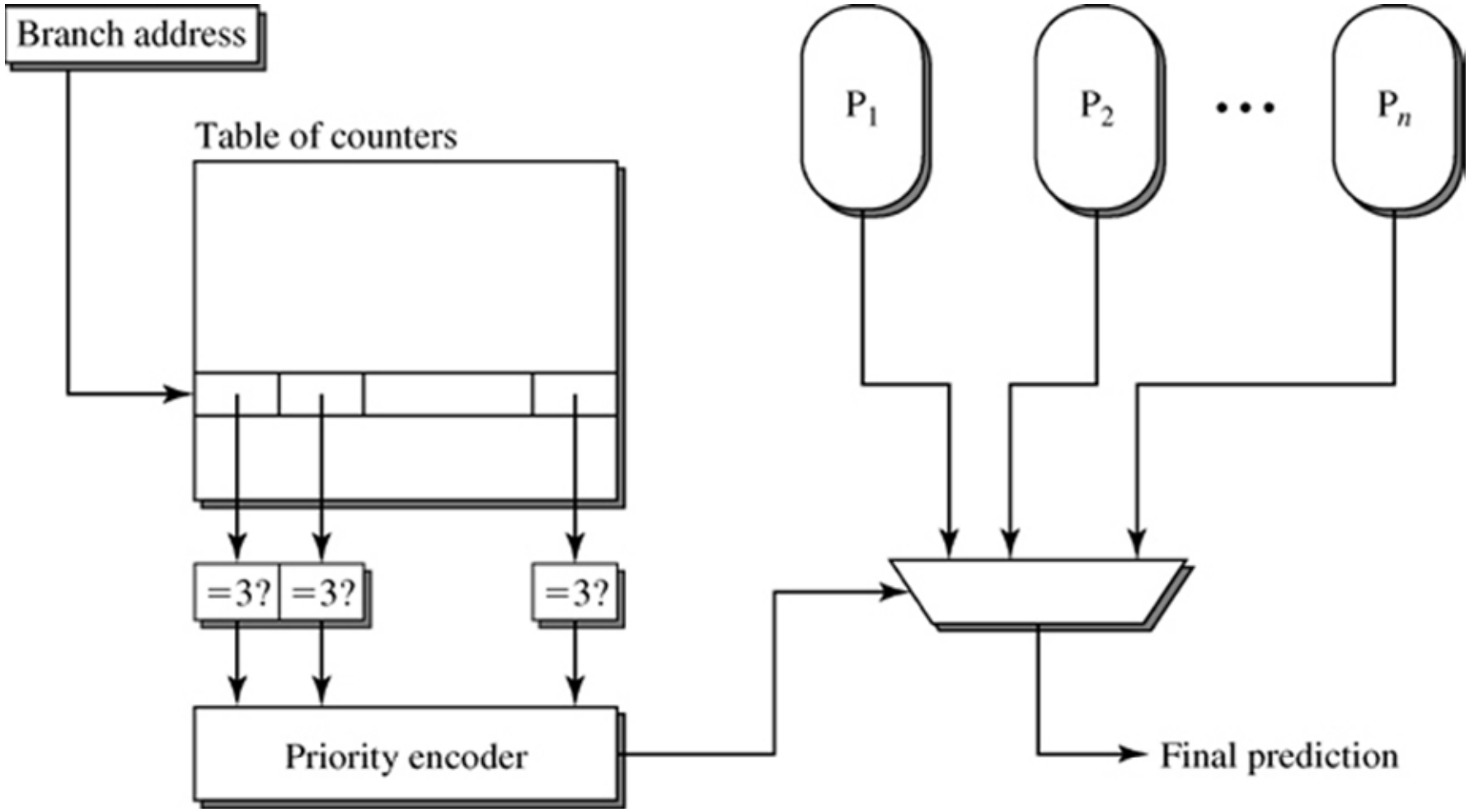

Figure 9.27: The Multihybrid Predictor.

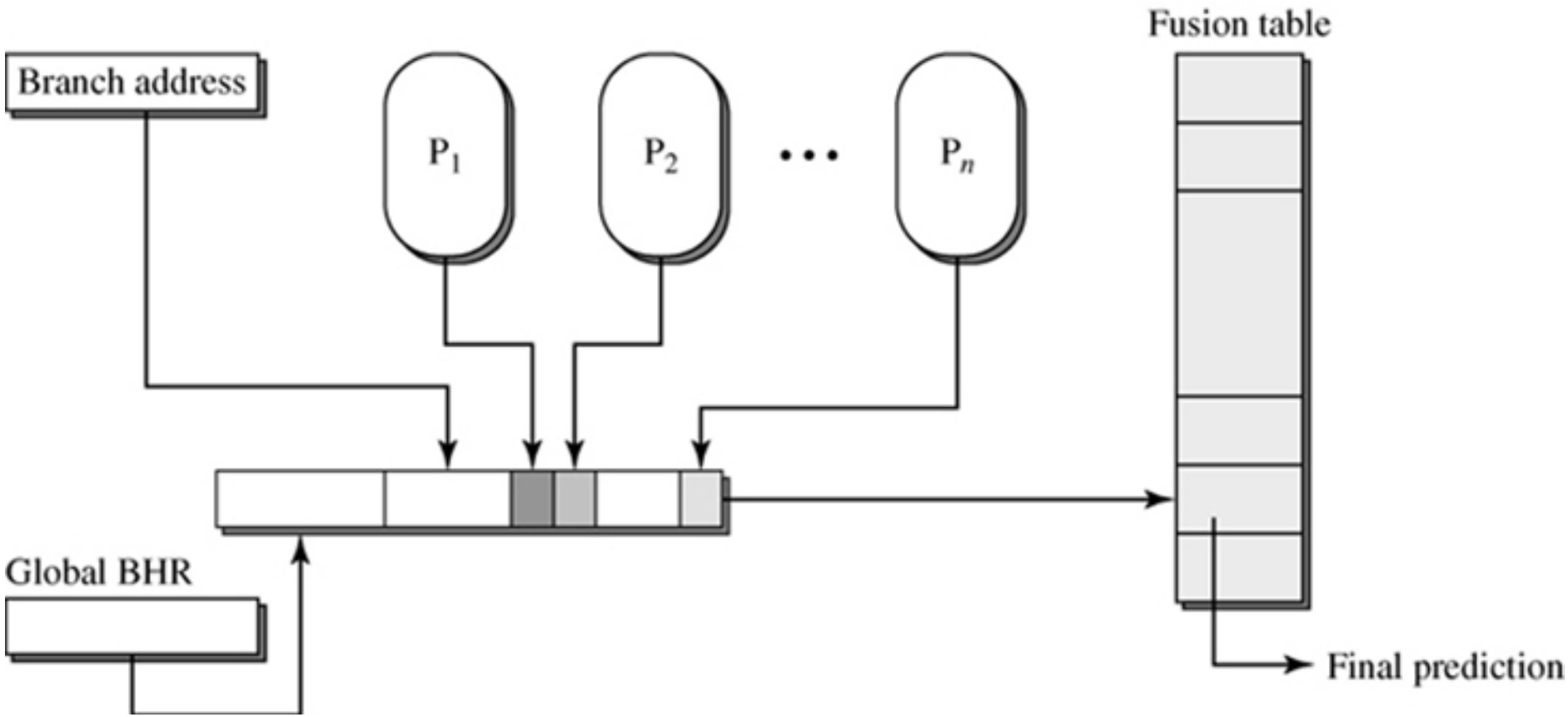

Figure 9.28: The Fusion Table Hybrid Predictor.

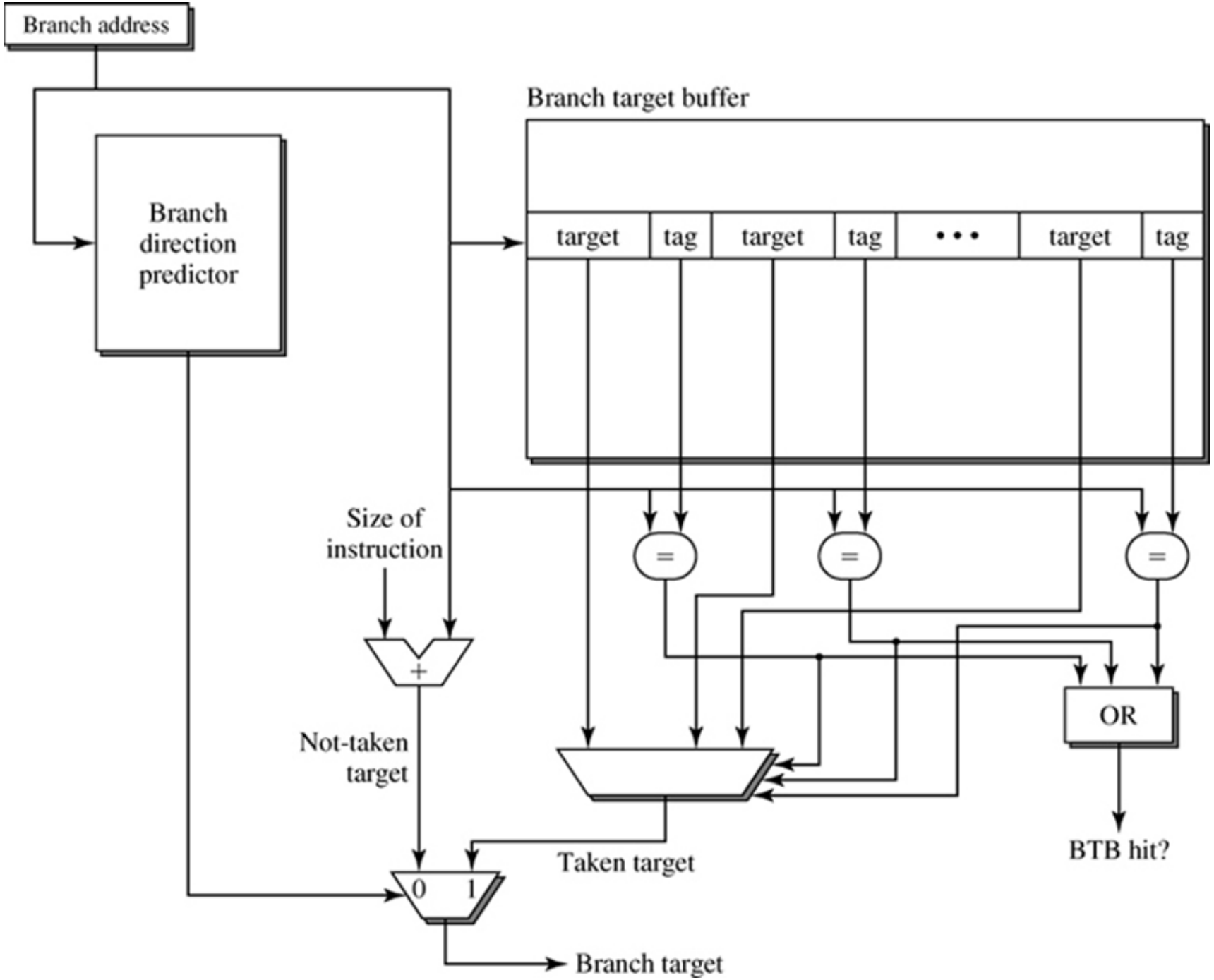

Figure 9.29: The Branch Target Buffer, a Generic Branch Predictor, and the Target Selection Logic.

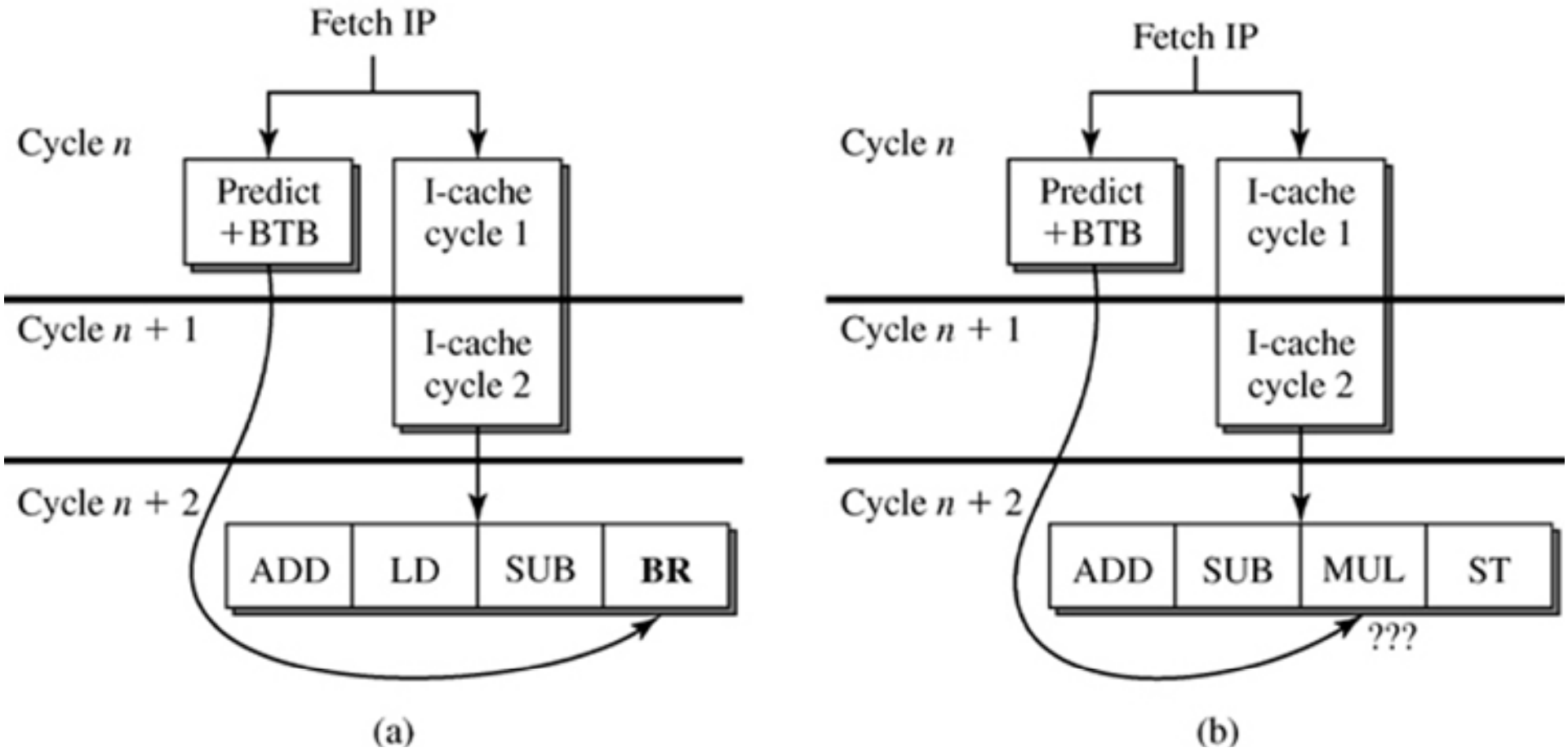

Figure 9.30: Timing Diagram Illustrating That a Branch Prediction Occurs before the Instruction Fetch Completes: (a) When a Branch is Present in the Fetch Block, and (b) When There is No Branch Present in the Fetch Block.

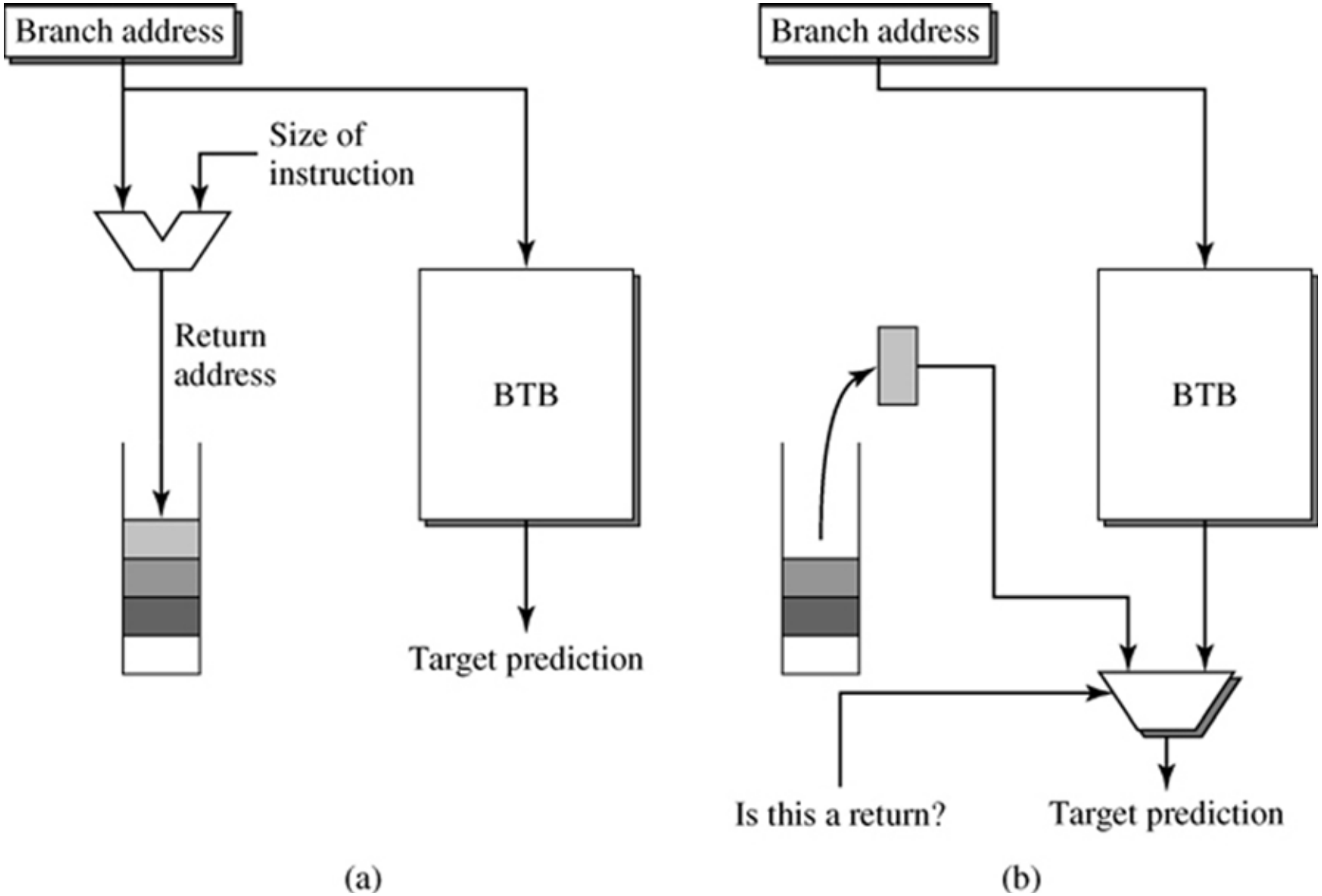

Figure 9.31: (a) Return Address Push on Jump to Subroutine. (b) Return Address Pop on Subroutine Return.

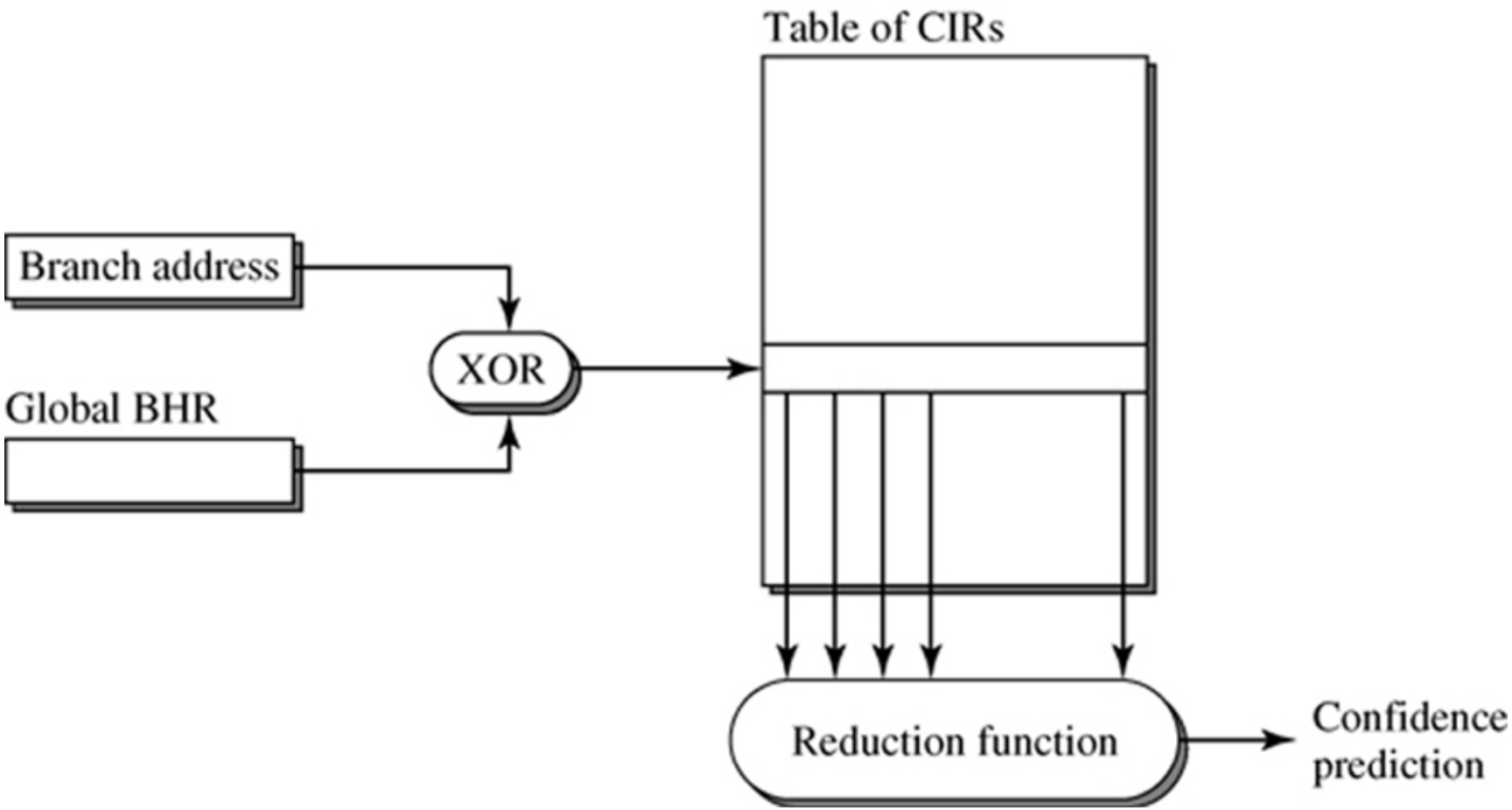

Figure 9.32: A Branch Confidence Predictor.

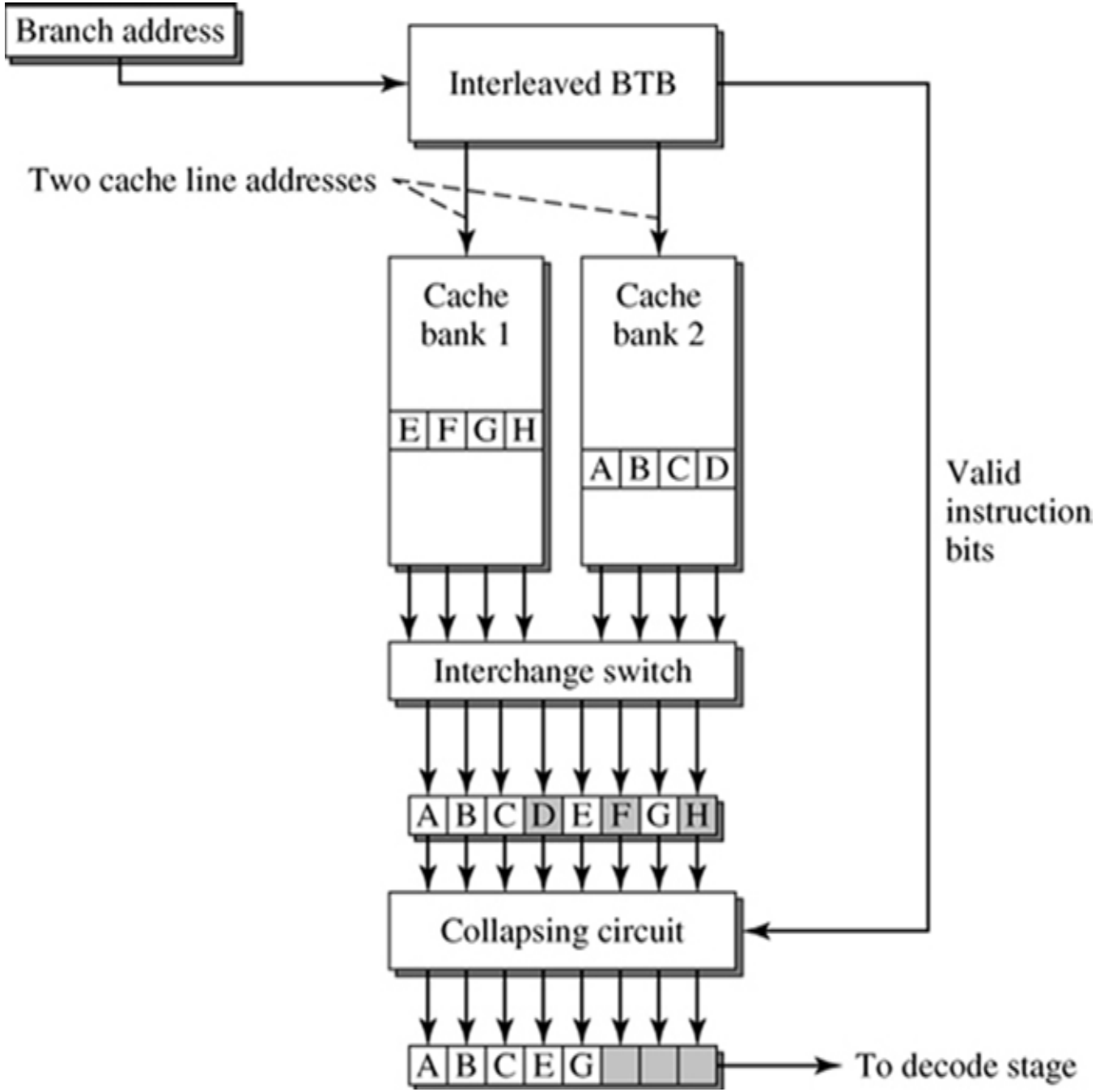

Figure 9.33: The Collapsing Buffer Fetch Organization.

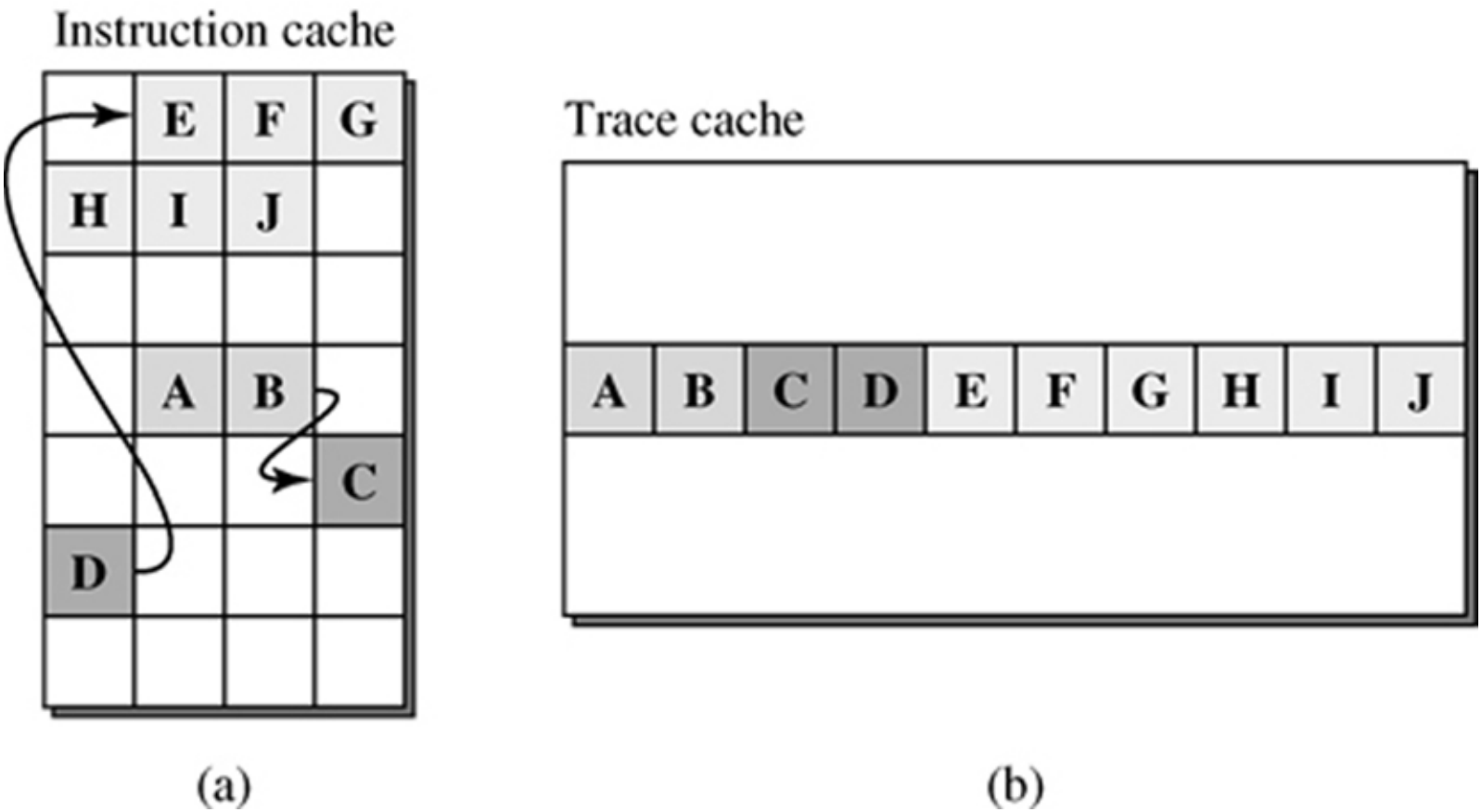

Figure 9.34: (a) Ten Instructions in an Instruction Cache. (b) The Same 10 Instructions in a Trace Cache.

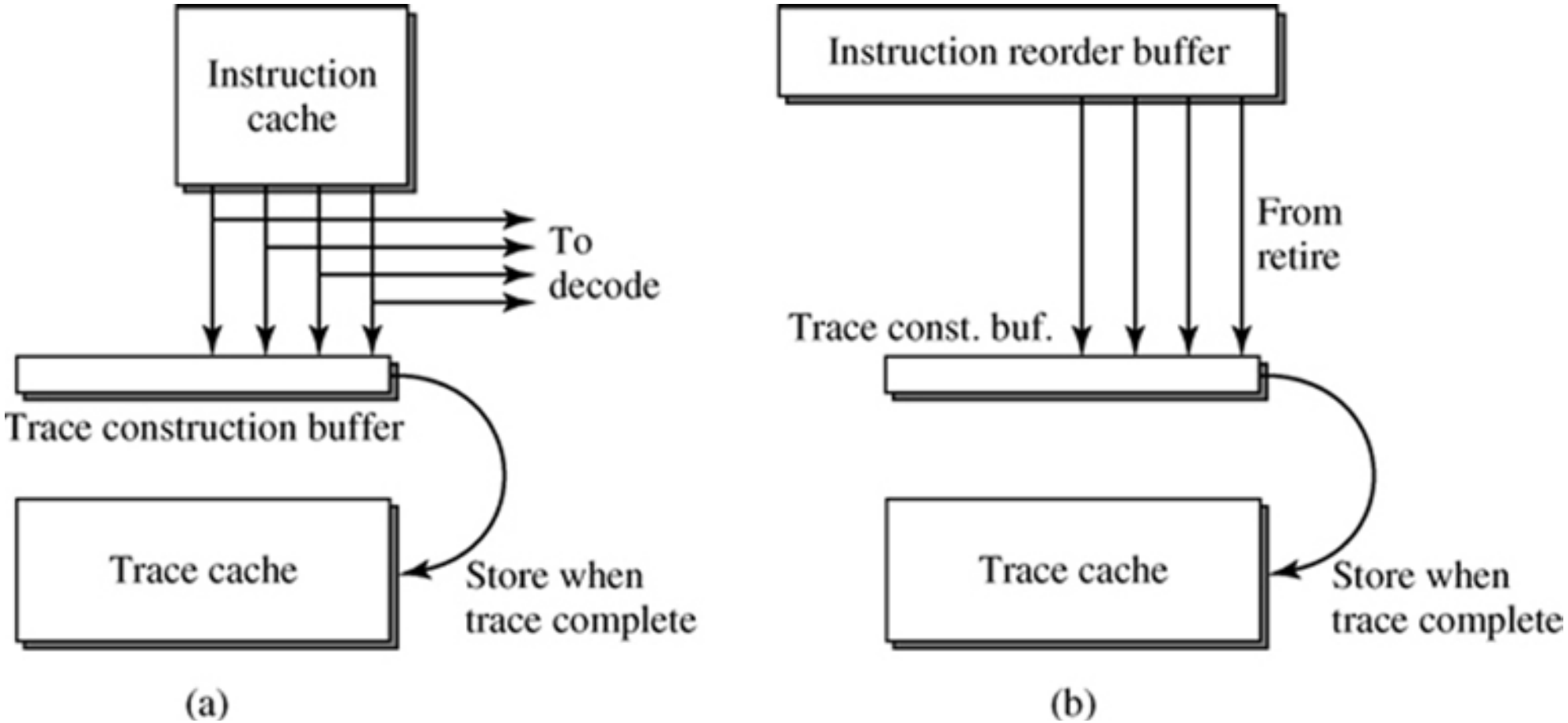

Figure 9.35: (a) Fetch-Time Trace Construction. (b) Completion-Time Trace Construction.

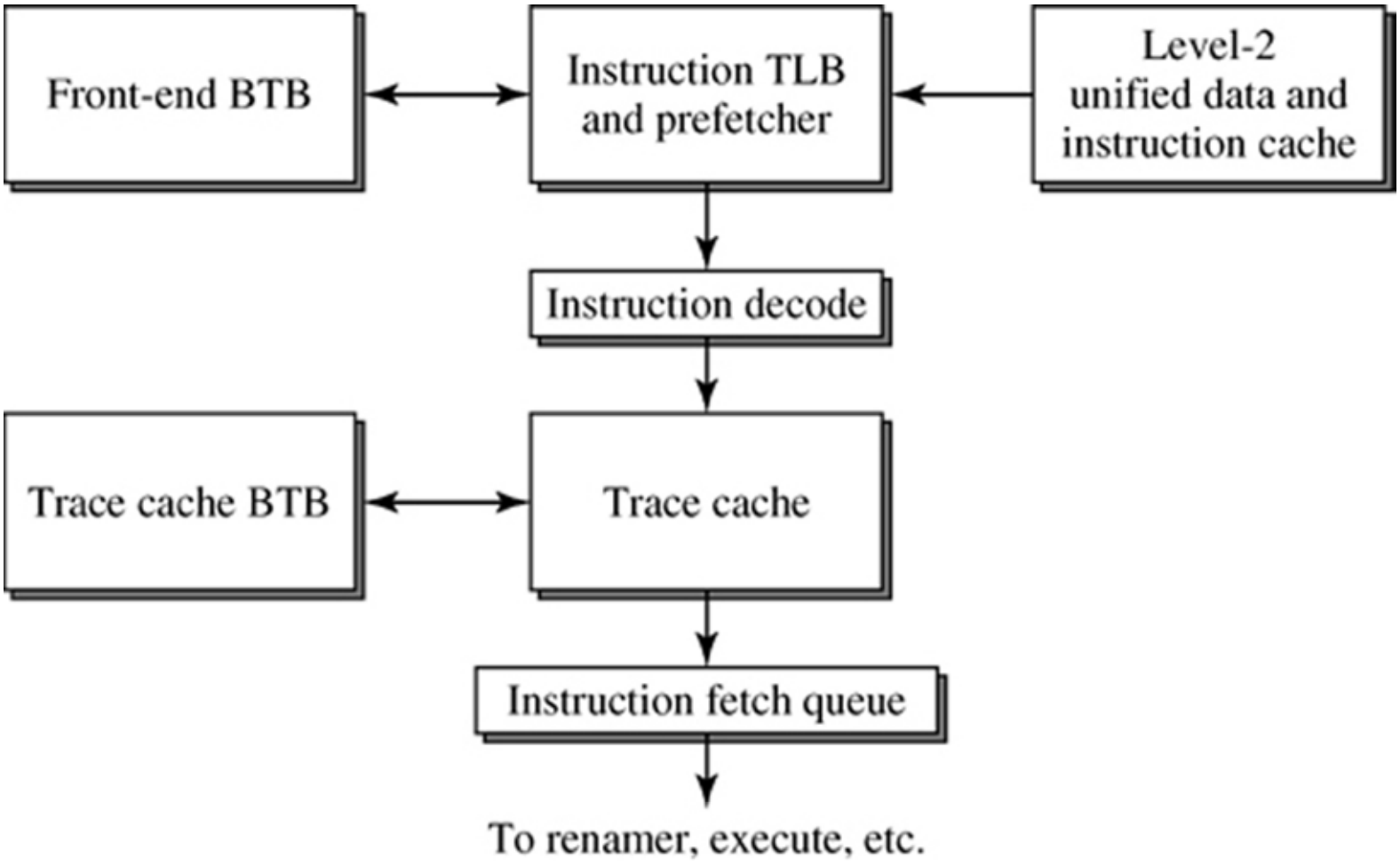

Figure 9.36: Intel Pentium 4 Trace Cache Organization.

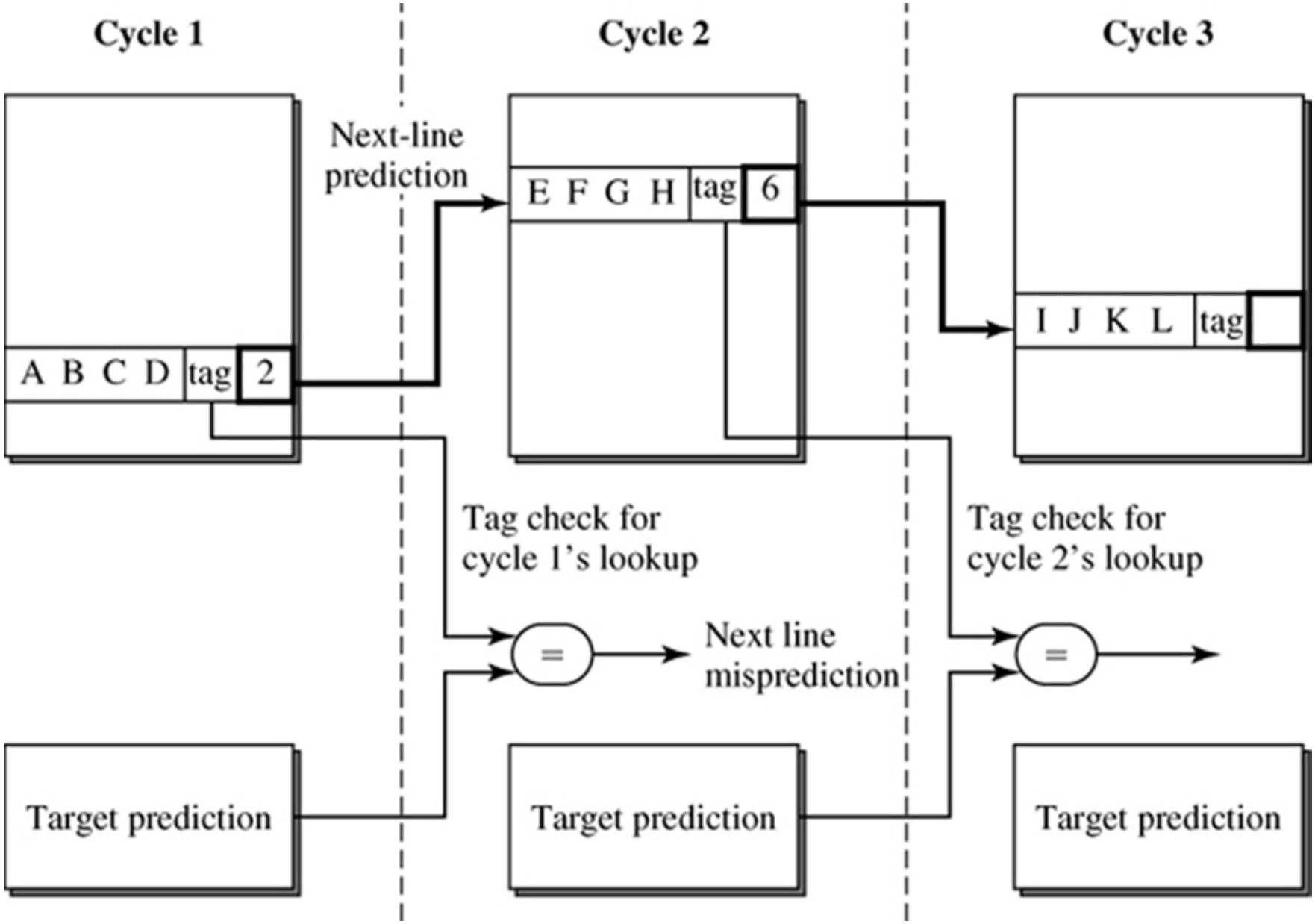

Figure 9.37: Direct-Mapped Cache with Next-Line Prediction.

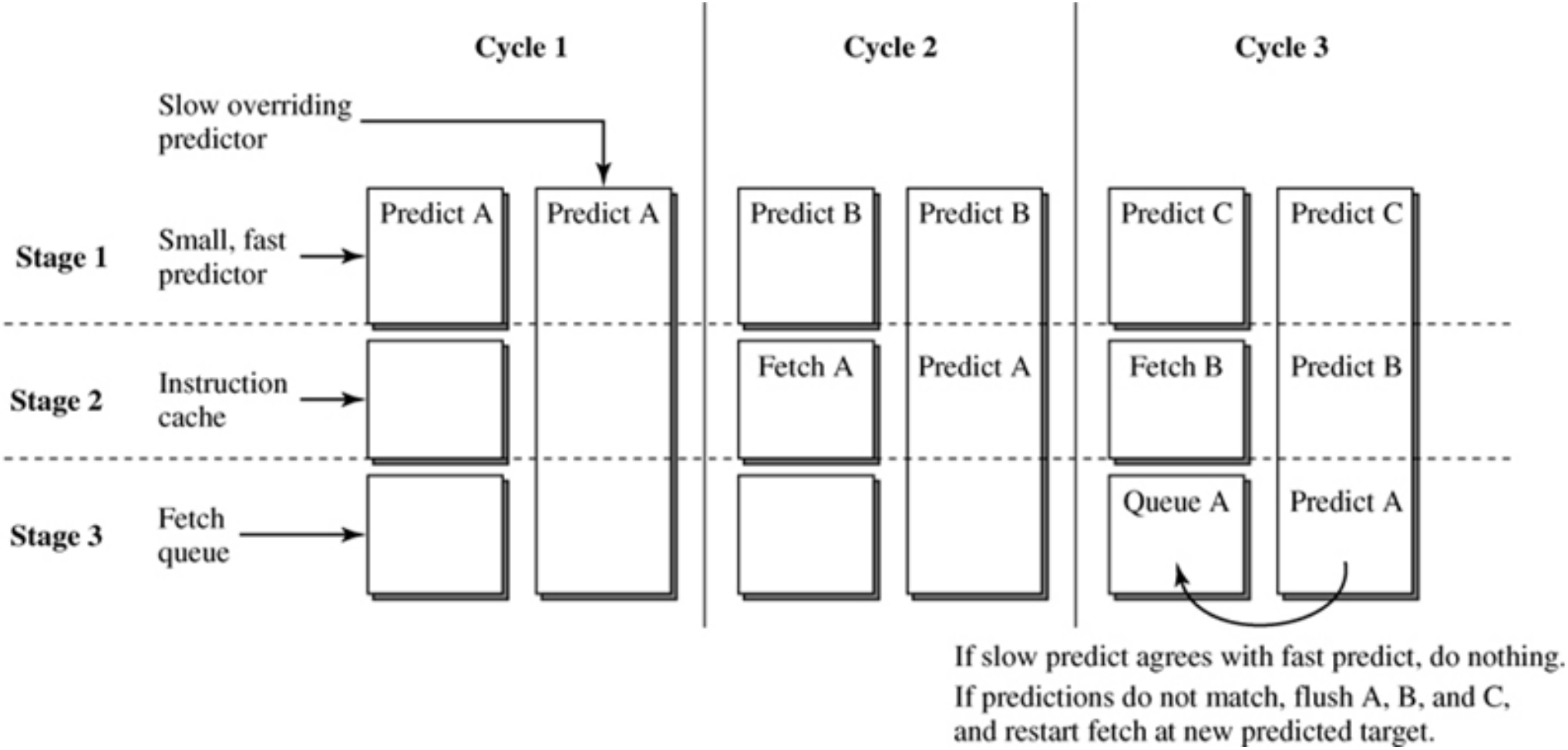

Figure 9.38: Organization of a Fast Predictor and a Slower Overriding Predictor.