

# EE485F Superscalar Processor Design: Syllabus

## Fall 2010

**Textbook** John Paul Shen and Mikko H. Lipasti, *Modern Processor Design: Fundamentals of Superscalar Processors*, McGraw Hill, 2005.

| Session # | Date      | Topic   | Reading Assignment | Homework Due              | Quizzes & Tests |
|-----------|-----------|---|--------------------|---------------------------|-----------------|
| 1         | 24-Aug-10 | Introduction  |                    |                           |                 |
| 2         | 25-Aug-10 | Instruction set design, measuring processor performance, instruction-level processing | Ch. 1              |                           |                 |
| 3         | 27-Aug-10 | Limits of instruction-level parallelism   |                    |                           |                 |
| 4         | 30-Aug-10 | Scalar pipelines  | Ch. 2              | P1.6, P1.12, P1.15        |                 |
| 5         | 1-Sep-10  | Ideal pipelining, instruction pipelining  |                    |                           |                 |
| 6         | 3-Sep-10  | Unifying instruction types  |                    |                           |                 |
|           | 6-Sep-10  | Labor Day Holiday   |                    |                           |                 |
| 7         | 8-Sep-10  | Deeply pipelined processors   |                    | P2.2, P2.13, P2.17        | Quiz 1          |
| 8         | 10-Sep-10 | Memory latency and bandwidth  | Ch. 3              |                           |                 |
| 9         | 13-Sep-10 | Temporal and spatial locality   |                    |                           |                 |
| 10        | 15-Sep-10 | Hierarchical memory systems and cache memory systems                                  |                    |                           |                 |
| 11        | 17-Sep-10 | Virtual memory  |                    |                           |                 |
| 12        | 20-Sep-10 | I/O Systems   |                    | P3.1, P3.16, P3.24        |                 |
| 13        | 22-Sep-10 | Limitations of scalar pipelines   | Ch. 4              |                           |                 |
| 14        | 24-Sep-10 | Parallel, diversified, and dynamic pipelines  |                    |                           |                 |
| 15        | 27-Sep-10 | Superscalar pipelines   |                    | P4.8, P4.10, P4.11, P4.12 |                 |
| 16        | 29-Sep-10 | Test I  |                    |                           | Test I          |
| 17        | 1-Oct-10  | Program control flow, control dependencies, and the effect of branch misprediction.   | Ch. 5              |                           |                 |
| 18        | 4-Oct-10  | Branch prediction techniques  |                    |                           |                 |
| 19        | 6-Oct-10  | Branch misprediction recovery   |                    |                           |                 |
| 20        | 8-Oct-10  | Register reuse and false data dependence  |                    |                           | Quiz 2          |
|           | 11-Oct-10 | Columbus Day Holiday  |                    |                           |                 |
| 21        | 13-Oct-10 | Register renaming techniques  |                    | P5.1, P5.2, P5.3          |                 |
| 22        | 15-Oct-10 | True data dependence, the data-flow limit   |                    |                           |                 |
| 23        | 18-Oct-10 | The Tomasulo algorithm for honoring true dependences                                  |                    |                           |                 |
| 24        | 20-Oct-10 | Dynamic instruction core, reservation stations, reorder buffers                       |                    | P5.4, P5.5, P5.6          |                 |
| 25        | 22-Oct-10 | Memory accessing instructions, ordering memory accesses                               |                    |                           |                 |
| 26        | 25-Oct-10 | Load bypassing, load forwarding   |                    |                           |                 |
| 27        | 27-Oct-10 | PowerPC620 Case Study I   | Ch. 6              |                           |                 |
| 28        | 29-Oct-10 | PowerPC620 Case Study II  |                    |                           |                 |
| 29        | 1-Nov-10  | PowerPC620 Case Study III   |                    | P6.8                      |                 |
| 30        | 3-Nov-10  | Test II   |                    |                           | Test II         |
| 31        | 5-Nov-10  | Intel P6 Case Study I   | Ch. 7              |                           |                 |
| 32        | 8-Nov-10  | Intel P6 Case Study II  |                    |                           |                 |
| 33        | 10-Nov-10 | Intel P6 Case Study III   |                    |                           |                 |
| 34        | 12-Nov-10 | Static Branch Prediction  | Ch. 9              |                           |                 |
| 35        | 15-Nov-10 | Dynamic branch prediction   |                    | P7.5                      |                 |
| 36        | 17-Nov-10 | Hybrid branch prediction  |                    |                           |                 |
| 37        | 19-Nov-10 | Other instruction flow techniques   |                    |                           |                 |
| 38        | 22-Nov-10 | Value locality and redundant execution  | Ch. 10             |                           | Quiz 3          |
| 39        | 24-Nov-10 | Memoization, instruction reuse, block and trace reuse                                 |                    |                           |                 |
|           | 26-Nov-10 | Thanksgiving Day Holiday  |                    |                           |                 |
| 40        | 29-Nov-10 | Data flow region reuse, weak dependence model, speculative value prediction           |                    |                           |                 |
| 41        | 1-Dec-10  | Introduction to multiprocessor systems  | Ch. 11.3           | P9.2, P9.3, P9.8          |                 |
| 42        | 3-Dec-10  | Cohere memory and cache structures  |                    |                           |                 |
| 43        | 6-Dec-10  | Student project presentations   |                    |                           |                 |
| 44        | 8-Dec-10  | Student project presentations   |                    | P10.8                     |                 |
| 45        | 10-Dec-10 | Review and course critique  |                    |                           |                 |