

COM-1001 BPSK/QPSK/OQPSK DEMODULATOR

Key Features

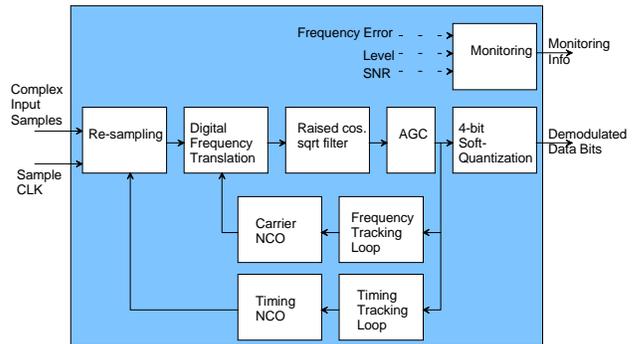
- Digital BPSK/QPSK Demodulator.
- Variable data rates up to 20 Mbps (QPSK) / 10 Mbps (BPSK).
- Differential / non-differential decoding.
- Includes raised cosine square root filter with 20%, 25%, or 40% rolloff options.
- Demodulation losses less than 0.5 dB with respect to theory at $E_b/N_0 = 1$ dB.
- Demodulation threshold < -2 dB E_b/N_0 .
- Frequency acquisition range: $\pm 50\%$ of the symbol rate.
- 4-bit soft-quantized demodulated bits.
- Extensive monitoring:
 - Carrier lock
 - Frequency error
 - AGC gain
 - SNR
- Connectorized 3"x 3" module for ease of prototyping. Standard 40 pin 2mm dual row connectors (left, right, bottom). Single 5V supply. Interfaces with 5V and 3.3V logic.

For the latest data sheet, please refer to the **ComBlock** web site: www.comblock.com/download/com1001.pdf. These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to www.comblock.com/product_list.htm.

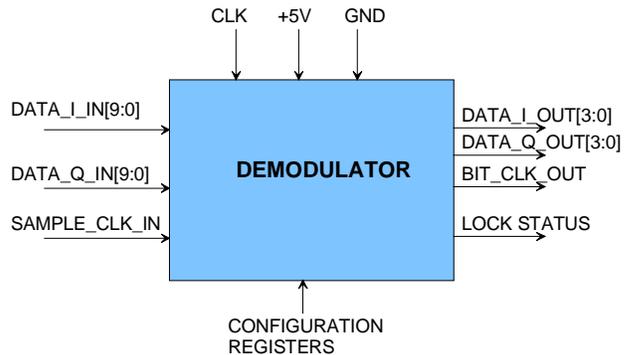


Block Diagram



Electrical Interface

Demodulator Inputs / Outputs



Input Module Interface	Definition
DATA_I_IN[9:0]	Modulated input signal, real axis. 10-bit precision. Format: 2's complement or unsigned. Unused LSBs are pulled low.
DATA_Q_IN[9:0]	Modulated input signal, imaginary axis. 10-bit precision. Same format as DATA_I_IN. Unused LSBs are pulled low.
SAMPLE_CLK_IN	Input signal sampling clock. One CLK-wide pulse. Read the input signal at the rising edge of CLK when SAMPLE_CLK_IN = '1'.

	Nominal sampling rate is between 4 and 8 samples per symbol. Samples can be consecutive. Signal is pulled-up.
AGC_OUT	Output. When this demodulator is connected directly to an analog receiver, it generates a pulse-width modulated signal to control the analog gain prior to A/D conversion. The purpose is to use the maximum dynamic range while preventing saturation at the A/D converter. 0 is the maximum gain, +3V is the minimum gain.
Output Module Interface	Definition
DATA_I_OUT[3:0]	4-bit soft-quantized demodulated bits, real axis. Unsigned representation: 0000 for maximum amplitude '0', 1111 for maximum amplitude '1'. When the serial output mode is selected, I and Q samples are transmitted one after another on this interface. I is transmitted before Q.
DATA_Q_OUT[3:0]	4-bit soft-quantized demodulated bits, imaginary axis. Same format as DATA_I_OUT. When the serial output mode is selected, this interface is unused.
BIT_CLK_OUT	Demodulated bit clock. One CLK-wide pulse. Read the output signal at the rising edge of CLK when BIT_CLK_OUT = '1'.
CARRIER_LOCK	'1' when the demodulator is locked, '0' otherwise.
Serial Monitoring & Control	DB9 connector. 115 Kbaud/s. 8-bit, no parity, one stop bit. No flow control.
Power Interface	4.75 – 5.25VDC. Terminal block. Power consumption is approximately proportional to the CLK frequency. The maximum power consumption at 40 MHz is 300mA.

Configuration (via Serial Link / LAN)

Complete assemblies can be monitored and controlled centrally over a single serial or LAN connection.

The module configuration parameters are stored in non-volatile memory. All control registers are read/write.

Parameters	Configuration
Nominal symbol rate x 4 (fsymbol rate x 4)	24-bit signed integer (2's complement) expressed as fsymbol rate x 4 * 2 ²³ / fs, where fs is the input sampling rate. Maximum recommended value: 2 ²³ – 1% margin (input sampling is near 4*symbol rate) Minimum recommended value: 2 ²² (input sampling is 8* symbol rate). Lower values are possible, but may result in aliasing depending on the input spectrum. REG0 = bit 7-0 REG1 = bit 15 – 8 REG2 = bit 23 – 16
Nominal carrier center frequency (fc)	24-bit signed integer (2's complement) expressed as fc * 2 ²⁴ / fsymbol rate x 4. Maximum range to avoid aliasing is +/- 1.5*fsymbol rate. REG3 = bit 7 – 0 REG4 = bit 15 – 8 REG5 = bit 23 - 16
Input sample format	0 = 2's complement 1 = unsigned REG6 bit 1
Carrier frequency tracking loop gain	0 = nominal 1 = 2x loop gain 2 = 4x loop gain 3 = 8x loop gain REG6 bits 3-2
Spectrum inversion	Invert Q bit. 0 = off 1 = on REG6 bit 5
Differential decoding	0 = off 1 = on REG6 bit 6
Freeze monitoring data	As the monitoring data is constantly changing, it is important to be able to prevent changes while reading a multi-byte parameter. Write a zero in bit 7 to freeze the monitoring data prior to reading it. Write a one to re-enable the update. REG6 bit 7
Output sample format	00 = I/Q parallel 01 = I/Q serial, I before Q (never use with BPSK as there is no information data on the Q channel) REG7 bits 1-0
Modulation	00 = BPSK 01 = QPSK 10 = OQPSK (I channel is delayed by ½ a symbol w.r.t. the Q channel) REG7 bit 5 – 4

Monitoring (via Serial Link / LAN)

Monitoring registers are read-only.

Parameters	Monitoring
Version	Returns '1001xy' when prompted for version number, where x is the firmware option and y the version.
Carrier frequency offset	Residual frequency offset with respect to the nominal carrier frequency. 24-bit signed integer (2's complement) expressed as $f_{\text{cdelta}} * 2^{24} / f_{\text{symbol rate}} * 4$ REG8 = bit 7 – 0 REG9 = bit 15 – 8 REG10 = bit 23 – 16
AGC gain	Digital AGC gain settings 8 bit unsigned REG11 bit 7-0.
NSR	Noise to signal ratio. Variance of the 4-bit soft-quantized demodulated samples at the optimum sampling instant averaged over 4096 symbols. Non-linear scale. Approximates 1/SNR. A few reference points: NSR = 24 -> SNR = 8.6 dB NSR = 34 -> SNR = 5.6 dB 8 bit unsigned. REG12 bits 7 – 0
Lock status	REG13 bit 0 0 = unlocked 1 = locked
I sample	I sample after digital AGC. Format: 8-bit 2's complement. This monitoring point can be used in conjunction with the Q sample to plot a scatter diagram. REG14 bits 7-0
Q sample	I sample after digital AGC. Format: 8-bit 2's complement. This monitoring point can be used in conjunction with the Q sample to plot a scatter diagram. REG15 bits 7-0

Default configuration at manufacturing:

REG0 = 0x00
REG1 = 0x00
REG2 = 0x40
REG3 = 0x00
REG4 = 0x00
REG5 = 0x00
REG6 = 0x82
REG7 = 0x00

Configuration example:

REG0 = 0x52
REG1 = 0xB8
REG2 = 0x7E
REG3 = 0x00
REG4 = 0x00
REG5 = 0x00
REG6 = 0x80
REG7 = 0x11

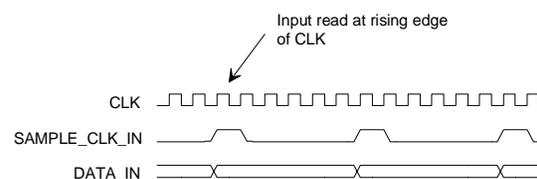
configures the demodulator as follows:
symbol rate x 4 = 39.6 MHz
offset carrier = 0 Hz
2's complement input format
nominal loop gain
no spectrum inversion
no differential decoding
serial output
QPSK

Timing

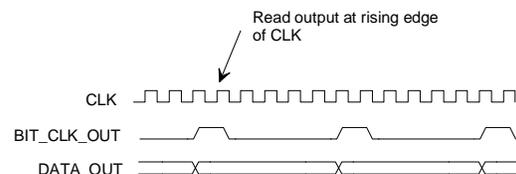
The I/O signals are synchronous with the rising edge of the reference clock CLK (i.e. all signals transitions always occur after the rising edge of the reference clock CLK). The maximum CLK frequency is 40 MHz.

The maximum demodulated data rate is equal to half of the reference clock frequency.

Input



Output



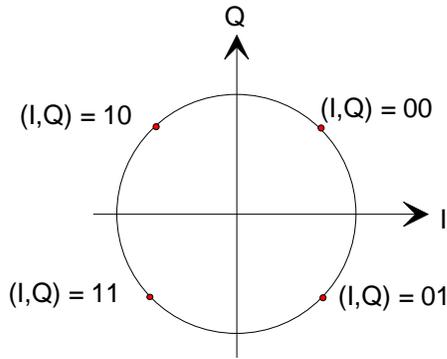
Test Points

Test points are provided for easy access by an oscilloscope probe.

Test Point	Definition
TP1	Carrier lock. Lock status is based on the rms phase error. This test point can be ambiguous as a 'no input signal' condition may yield be confused as carrier lock. Use in conjunction with bit transition (TP7) to remove any ambiguity.
TP2	Frequency acquisition in progress
TP3	Recovered carrier
TP4	Recovered timing (2*symbol rate)
TP5	Demodulated bit, I-channel DATA_I_OUT(3)
TP6	Demodulated bit, Q-channel DATA_Q_OUT(3)
TP7	Bit transitions. '1' if at least symbol transition within any 1023 symbol window.

Implementation

Phase Map (QPSK)



As with all QPSK demodulators, there is a phase ambiguity of $n \cdot 90$ deg in the demodulated output. The phase ambiguity is not resolved in this module. It is typically resolved either through the use of a unique word periodically inserted in the data stream (for example when using Turbo code or Reed-Solomon block code) or through bit error rate detection in Viterbi decoder.

Differential Decoding (QPSK)

In low data rate applications where the phase noise can affect the bit error rate performances, it can be advisable to use differential QPSK. The phase difference between two successive symbols conveys the information symbol.

0 deg = "00"
 90 deg = "01"
 180 deg = "10"
 270 deg = "11".

This implementation is not strictly that of a DPSK demodulator in the sense that the receiver still tracks the carrier phase and frequency using a Costas loop.

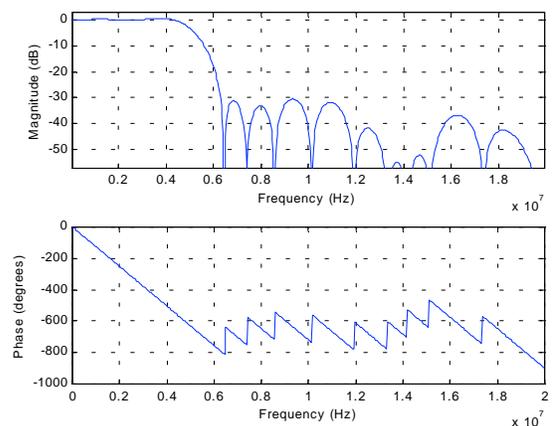
Filter Response

This module is configured at installation with a 20% rolloff filter. The filter rolloff can be selected among 20%, 25% and 40%. Changing the rolloff selection requires re-loading the firmware using the ComBlock control center.

The three firmware versions can be downloaded from www.comblock.com/download.

- COM-1001-A QPSK demodulator 20% rolloff
- COM-1001-B QPSK demodulator 25% rolloff
- COM-1001-E QPSK demodulator 40% rolloff

Filter Response (20% rolloff)



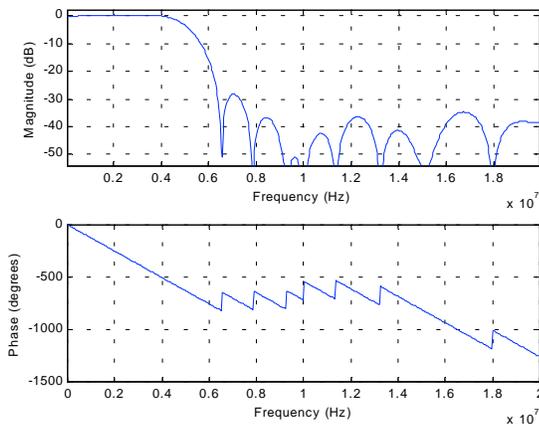
(filter response normalized for 4*symbol rate = 40 MHz)

The raised cosine square root filter with 20% rolloff is a 29-tap FIR filter with the following impulse response:

Coeff(0) = -8/1024
 Coeff(1) = -16/1024
 Coeff(2) = -8/1024

Coeff(3) = 8/1024
 Coeff(4) = 24/1024
 Coeff(5) = 24/1024
 Coeff(6) = 12/1024
 Coeff(7) = -16/1024
 Coeff(8) = -48/1024
 Coeff(9) = -52/1024
 Coeff(10) = -16/1024
 Coeff(11) = 64/1024
 Coeff(12) = 160/1024
 Coeff(13) = 240/1024
 Coeff(14) = 272/1024
 Coeff(j=15:28) = coeff(28-j);

Filter Response (25% rolloff)

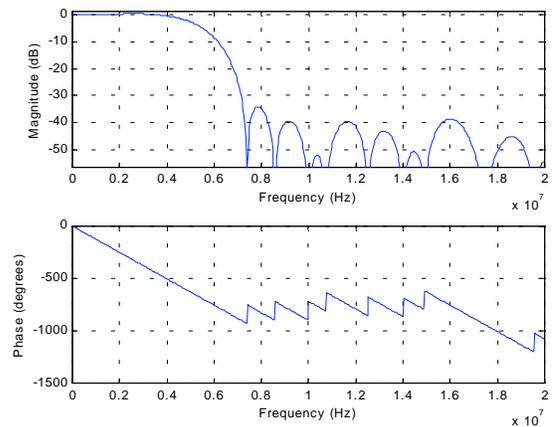


(filter response normalized for 4*symbol rate = 40 MHz)

The raised cosine square root filter with 25% rolloff is a 29-tap FIR filter with the following impulse response:

Coeff(0) = -4/1024
 Coeff(1) = -12/1024
 Coeff(2) = -8/1024
 Coeff(3) = 2/1024
 Coeff(4) = 16/1024
 Coeff(5) = 24/1024
 Coeff(6) = 12/1024
 Coeff(7) = -16/1024
 Coeff(8) = -48/1024
 Coeff(9) = -48/1024
 Coeff(10) = -16/1024
 Coeff(11) = 64/1024
 Coeff(12) = 160/1024
 Coeff(13) = 240/1024
 Coeff(14) = 272/1024
 Coeff(j=15:28) = coeff(28-j);

Filter Response (40% rolloff)



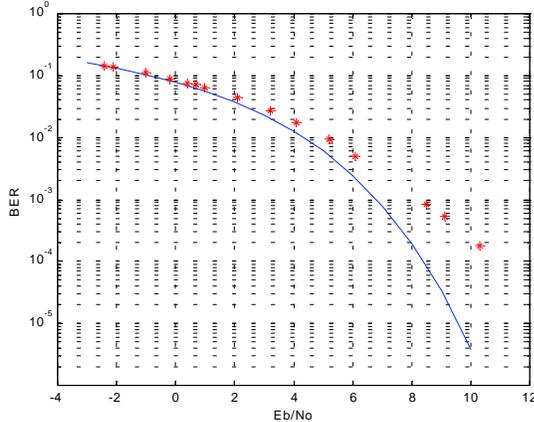
(filter response normalized for 4*symbol rate = 40 MHz)

The raised cosine square root filter with 40% rolloff is a 29-tap FIR filter with the following impulse response:

Coeff(0) = 4/1024
 Coeff(1) = 1/1024
 Coeff(2) = -4/1024
 Coeff(3) = -4/1024
 Coeff(4) = 2/1024
 Coeff(5) = 12/1024
 Coeff(6) = 14/1024
 Coeff(7) = -2/1024
 Coeff(8) = -30/1024
 Coeff(9) = -48/1024
 Coeff(10) = -24/1024
 Coeff(11) = 48/1024
 Coeff(12) = 152/1024
 Coeff(13) = 248/1024
 Coeff(14) = 284/1024
 Coeff(j=15:28) = coeff(28-j);

Bit Error Rate Performances

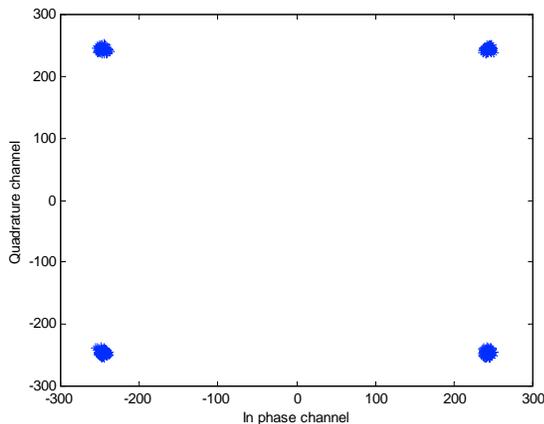
The demodulator bit-error-rate performances are within 0.5 dB from the theoretical performances $\frac{1}{2} * \text{erfc}(E_b/N_o)$ of QPSK demodulators at E_b/N_o . of 1 dB Actual measurements taken by using the COM-1001-E digital demodulator, the COM-1002-E digital modulator and the COM-1003 noise generator are shown below:



BER performance

The demodulator threshold is better than -2 dB E_b/N_o , during digital back to back tests.

The demodulated QPSK bits (also captured with back to back digital modulator-demodulator) . It shows that the intersymbol interferences are negligible.



Frequency Tracking

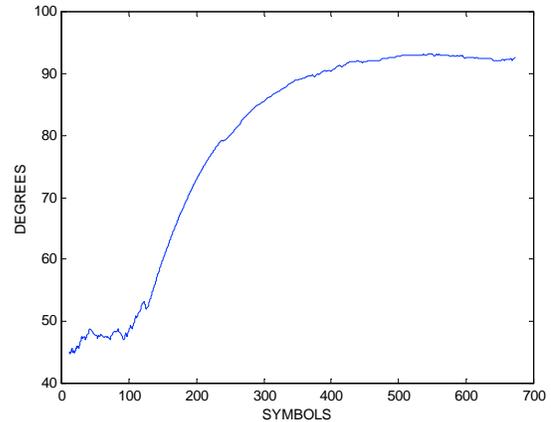
The carrier tracking loop is a second order loop. It can track the center frequency over a range of +/- 1.5 * symbol rate.

For high data rates (> 100 Kbps), carrier phase noise is generally negligible. For lower data rates, it is may be necessary to adjust the carrier tracking loop gain as a tradeoff between carrier phase noise (originating at the modulator, up-converter, down-converter, etc) and thermal noise. To this effect, the user is given control of the loop gain over a range of x1, x2, x4 and x8.

Frequency Acquisition

The carrier frequency loop nominal settings are selected to keep the BER degradations small (within 0.5 dB from theory) at the threshold SNR. The resulting frequency acquisition range is about 1% of the symbol rate. The acquisition time is typically 500 symbols as shown below.

The carrier tracking loop's response to a (worst case) 45 degrees phase error step at the input is shown below.



NCO phase response to a 45 deg. input phase error step. Nominal loop gain. Noiseless.

When an out-of-lock condition is detected, a fast acquisition algorithm is activated. This algorithm is capable of detecting and correcting center frequency errors of up to +/- 50% of the symbol rate. The algorithm relies on the spectrum symmetry: it is thus important to ensure bit randomness at the transmitter for a symmetrical spectrum.

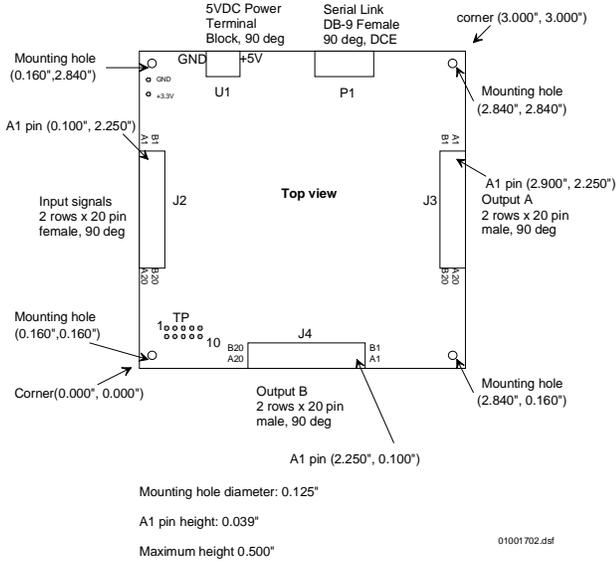
Input Interpolation

This module provides fine selection of symbol rates, as long as the input sampling rate is between x4 and x8 the symbol rate. For higher ratios between input sampling rate / symbol rate, the COM-1008 variable decimation filter is recommended to prevent aliasing.

AGC

A digital AGC provides 18 dB of dynamic range for signals following the raised cosine filter.

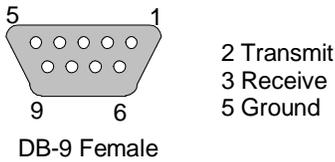
Mechanical Interface



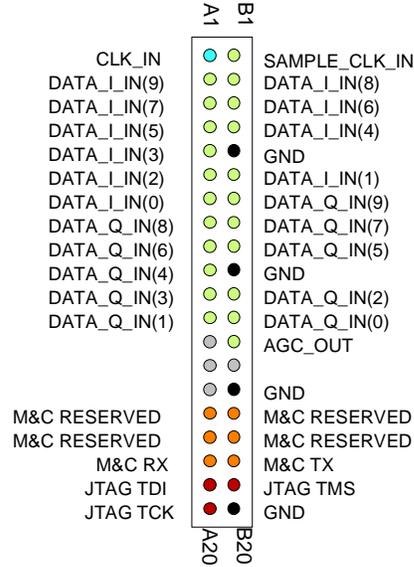
Pinout

Serial Link P1

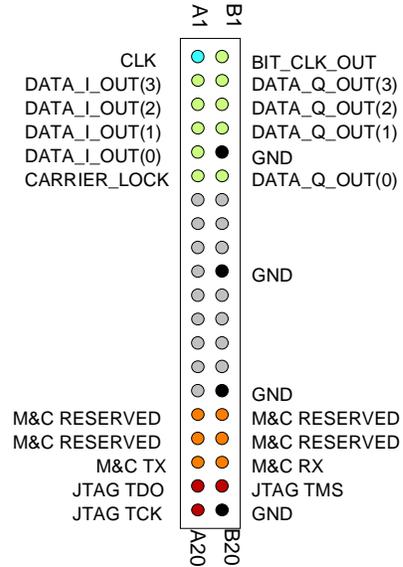
The DB-9 connector is wired as data circuit terminating equipment (DCE). Connection to a PC is over a straight-through cable. No null modem or gender changer is required.



Input Connector J2



Output Connectors J3, J4



I/O Compatibility List

(not an exhaustive list)

Input	Output
COM-1002 BPSK/QPSK/OQPSK modulator (digital back to back)	COM-1005 Bit Error Rate Measurement
COM-300x RF receivers	COM-7001 Turbo Code decoder
COM-1008 Variable decimation	COM-1009 Convolutional decoder K=5, 7
COM-1023 BER generator, AWGN generator	COM-1015 Convolutional decoder K=9
COM-1024 Multi-path generator	

ComBlock Ordering Information

COM-1001 Digital BPSK/QPSK/OQPSK
demodulator

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