EE332

Assignment 30

Digital Logic

Name: Master Oct 28, 2002

Section: 3311

1. Use a Karnaugh map to generate minimal logic for a function F which will be true (1) if its 4-bit input is in the range 7 to 11 (inclusive) or if it is evenly divisible by 4.

2. Manipulate the result so that it is implemented using 2-input NAND gates only. Draw a schematic for the resultant equation.

	A	B	C	D	F
0	0	0	0	0	1
1	0	0	0	1	
2	0	0	1	0	
3	0	0	1	1	
4	0	1	0	0	1
5	0	1	0	1	
6	0	1	1	0	
7	0	1	1	1	1
8	1	0	0	0	1
9	1	0	0	1	1
10	1	0	1	0	1
11	1	0	1	1	1
12	1	1	0	0	1
13	1	1	0	1	
14	1	1	1	0	
15	1	1	1	1	

F	CD 00	01	11	10
AB 00	1	0	0	0
01	1	0	1	0
11	1	0	0	0
10	1	1	1	1

$$F = A\bar{B} + \bar{C}\bar{D} + \bar{A}BCD$$

$$= \overline{A\bar{B} + \bar{C}\bar{D} + \bar{A}BCD}$$

$$= \overline{\overline{A\bar{B}}\ \overline{\bar{C}\bar{D}}\ \overline{\bar{A}BCD}}$$

$$= \overline{\overline{A\bar{B}}\ \overline{\bar{C}\bar{D}}\ \overline{\bar{A}B}\ \overline{CD}}$$

To get 2-input Nand gates only:
(1) Replace $\bar{x}$ by $\overline{x \cdot x}$.
(2) Replace $x+y$ by $\overline{\overline{x+y}} = \overline{\bar{x} \cdot \bar{y}}$
(3) Replace $x \cdot y$ by $\overline{\overline{x \cdot y}}$