

1. SHORT ANSWER:

- a. (10 pts) Express the following numbers in two's complement **6-bit notation**. If this is not possible, so state.

i. -31

ii. +53

100001Not possible $-31 = -(01111)$ $\overline{100001}$

- b. (10 pts) **10011** is a **5-bit signed two's complement binary representation**. What integer does it represent?

$$10011 = -(01101) = -13$$

- c. (10 pts) Convert 10.8_{16} to decimal

$$10_{16} = 32_{10}$$

$$\text{So } 10.8_{16} = 32.5_{10}$$

$$0.8_{16} = \frac{8}{16} = \frac{1}{2}$$

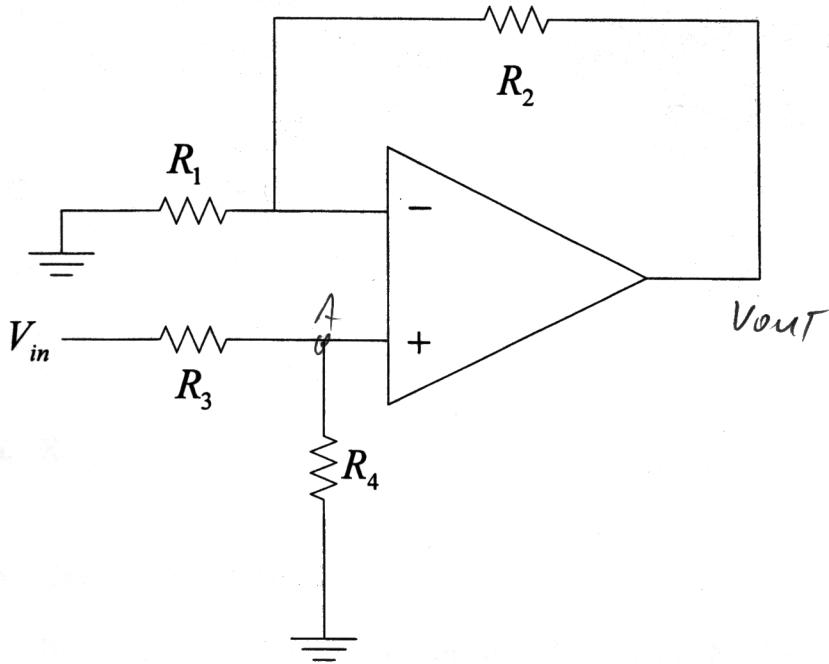
- d. (10 pts) **TRUE or FALSE:**

i. $A + \bar{A}B = A + B$ True

ii. $\bar{A}\bar{B} = \overline{A B}$ False

- e. (10 pts) The **Summing Point Constraint** used to analyze OPAMPS in EE332 requires negative feedback be present, the differential voltage must be zero, and input current must be zero.

2. (50 pts) Given the ideal OPAMP shown, if $R_1 = R_3 = 10\text{ k}\Omega$ and $R_4 = 50\text{ k}\Omega$ what must R_2 be to achieve a voltage gain of 1?



$$V_A = \frac{R_4}{R_3 + R_4} V_{in}$$

$$V_{out} = \left(1 + \frac{R_2}{R_1}\right) V_A$$

$$= \left(1 + \frac{R_2}{R_1}\right) \left(\frac{R_4}{R_3 + R_4}\right) V_{in}$$

$$R_2 = \left[\frac{V_{out}}{\left(\frac{R_4}{R_3 + R_4}\right) V_{in}} - 1 \right] R_1$$

$$R_2 = \left[\frac{1}{\frac{50\text{k}\Omega}{10\text{k}\Omega + 50\text{k}\Omega}} - 1 \right] 10\text{k}\Omega$$

$$= \left(\frac{6}{5} - \frac{5}{5} \right) 10\text{k}\Omega$$

$$= \frac{10\text{k}\Omega}{5}$$

$$= 2\text{k}\Omega$$

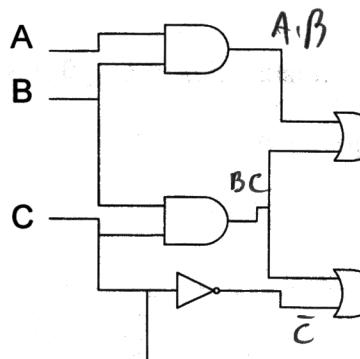
$$(A+C)B(B+\bar{C}) = (AB+BC)(B+\bar{C})$$

$$= AB + BC + ABC$$

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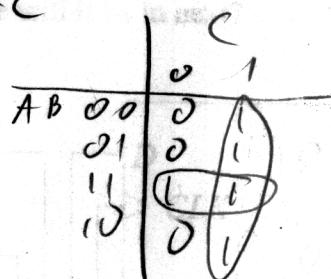
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3. (50 pts) Minimize the circuit utilizing Boolean algebra and Karnaugh Maps. Redraw the circuit and verify your answer using truth tables.



$$\begin{aligned} & A \cdot \bar{B} \\ & AB + BC \\ & BC \\ & \bar{C} \\ & BC + \bar{C} = B\bar{C} \end{aligned}$$

$$\begin{aligned} & (A+C)B(B+\bar{C}) \\ & = (A+C)B \\ & X = (A+C)B + C \\ & AB + BC + C \\ & = AB + C \end{aligned}$$

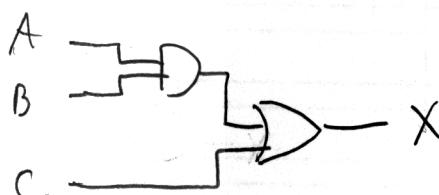


10 a. $X = \underline{BC}$

10 b. Draw the KMAP for X

10 c. Based on part b above, write the MSOP version of X. $X_{MSOP} = \underline{AB + C}$

d. Sketch the minimized circuit and show that it is equivalent to the circuit given.

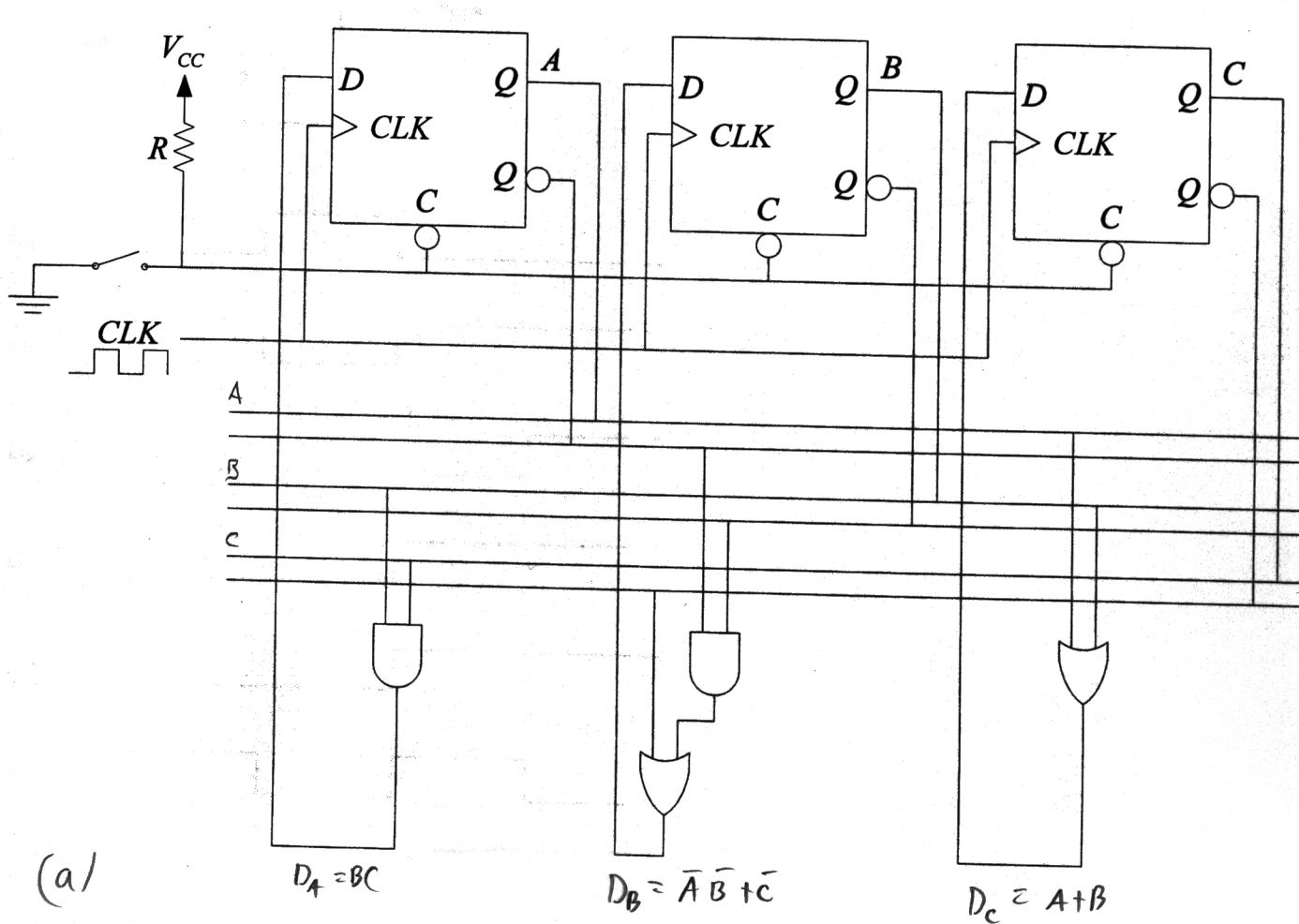


A	B	C	AB	BC	$AB + BC$	\bar{C}	$BC + \bar{C}$	$(AB + BC)(BC + \bar{C})$	$(AB + BC)(BC + \bar{C}) + C$	$AB + C$
0	0	0	0	0	0	1	1	0	0	0
0	0	1	0	0	0	0	0	0	0	1
0	1	0	0	0	0	1	1	0	0	0
0	1	1	0	1	1	0	1	1	1	1
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	0	0	0
1	1	0	1	0	1	1	1	1	1	1
1	1	1	1	1	1	0	1	1	1	1

= 5

4. (50 pts) Assume that the switch remains open at all times, as shown in the figure.

- Write the logic equations for D_A , D_B , and D_C
- If this circuit is in the state with $A = 0$, $B = 1$, and $C = 0$, what state will it be in next?
- If it is in the state with $A = 0$, $B = 0$, and $C = 1$, what state will it be in next?



(a)

$$D_A = BC$$

$$D_B = \bar{A}\bar{B}\bar{C}$$

$$D_C = A+B$$

(b)

$$010 \rightarrow 011$$

(3)

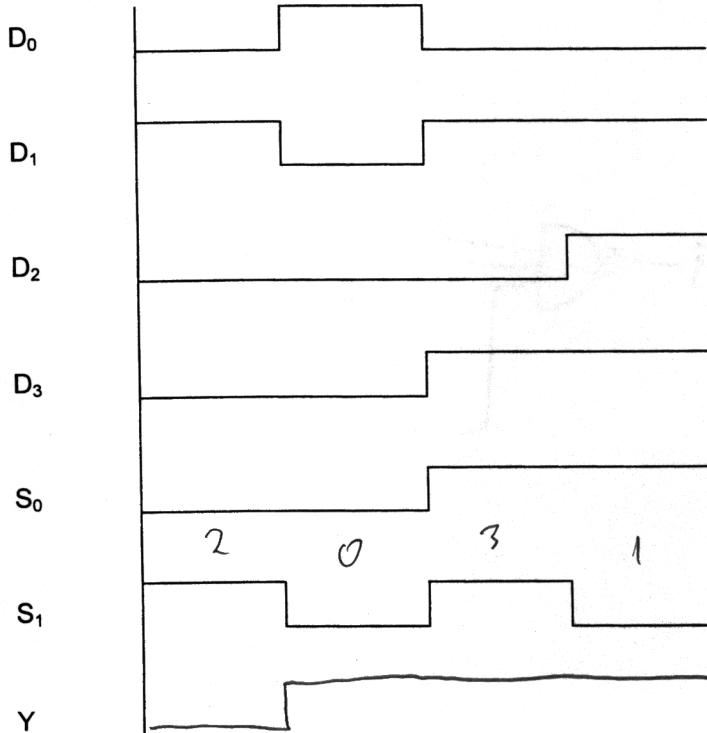
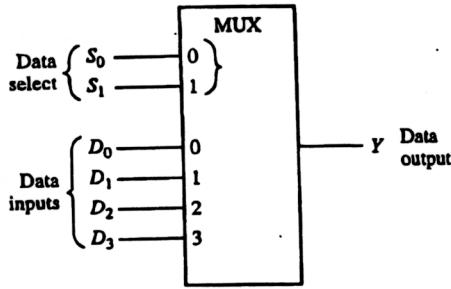
(c)

$$001 \rightarrow 010$$

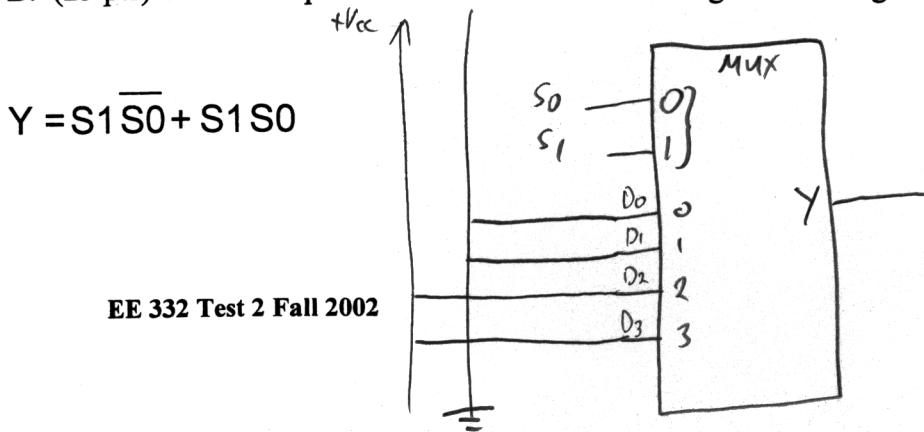
(2)

5. (50 pts)

A. (25 pts) Based on the 4:1 Multiplexer below and the input signals, determine the "Y" output



B. (25 pts) Utilize the previous MUX to realize the logic function given; sketch the diagram:



EXTRA CREDIT: (20 pts)Implement the following function using only NAND gates:

$$F = A + B + \bar{C}$$

$$\begin{aligned} F &= A + B + \bar{C} \\ &= \overline{\overline{A + B + \bar{C}}} \\ &= \overline{\overline{A} \overline{B} C} \end{aligned}$$

