

EE461 Microprocessor-based Digital Design

Spring 2005

Assignment 2 Solutions

Digital Logic Review

- Figure 1 contains a schematic for a sequential counter. Derive logic equations for the signals within it and fill in the timing diagram in the figure, assuming the state machines initial state is $ABC = 000$. If the state variables A , B , and C are interpreted as a three-bit binary number ABC , what pattern does the counter generate?

SOLUTION

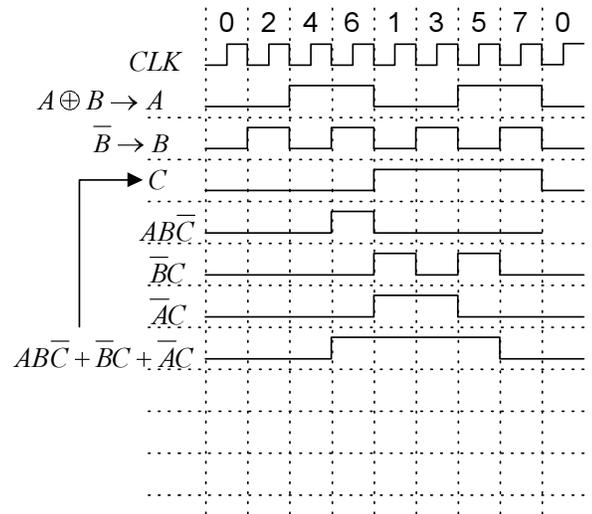
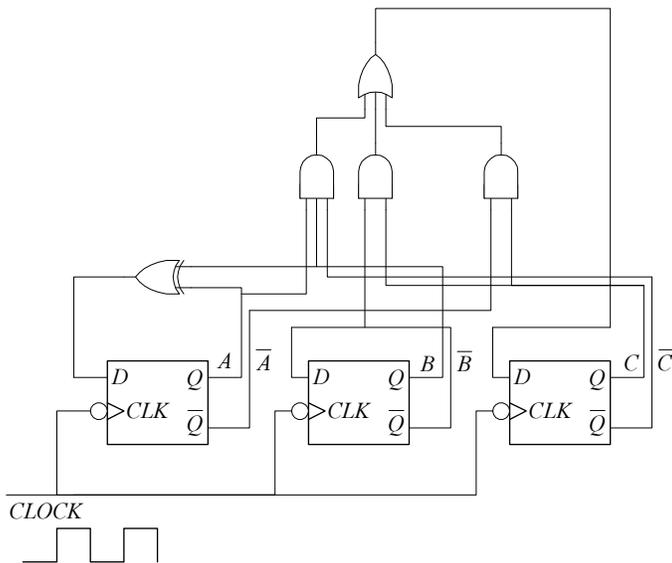


Figure 1: Schematic of a counter