

## 2.2.2.6 PIE2 REGISTER

The PIE2 register contains the individual enable bits for the CCP2 peripheral interrupt, the SSP bus collision interrupt, and the EEPROM write operation interrupt.

### REGISTER 2-6: PIE2 REGISTER (ADDRESS 8Dh)

U-0	R/W-0	U-0	R/W-0	R/W-0	U-0	U-0	R/W-0
—	—	—	EEIE	BCLIE	—	—	CCP2IE
bit7							bit0

R = Readable bit  
W = Writable bit  
U = Unimplemented bit, read as '0'  
- n= Value at POR reset

bit 7: **Unimplemented:** Read as '0'

bit 6: **Reserved:** Always maintain this bit clear

bit 5: **Unimplemented:** Read as '0'

bit 4: **EEIE:** EEPROM Write Operation Interrupt Enable  
1 = Enable EE Write Interrupt  
0 = Disable EE Write Interrupt

bit 3: **BCLIE:** Bus Collision Interrupt Enable  
1 = Enable Bus Collision Interrupt  
0 = Disable Bus Collision Interrupt

bit 2-1: **Unimplemented:** Read as '0'

bit 0: **CCP2IE:** CCP2 Interrupt Enable bit  
1 = Enables the CCP2 interrupt  
0 = Disables the CCP2 interrupt