

EE462 Test #2: 30 OCT 2001

4. (30 pts) Design a decoder circuit to generate the signals ROM (active low) and RAM (active high) for the following memory map used in a C31-based system. Your design may use just AND, NAND, OR, NOR, and NOT gates. Be sure to include appropriate control signals in your design.

Device type	Address range	Permissible operations
ROM	0C0000h - 0FFFFFFh	Read only
RAM	100000h - 1FFFFFFh	Read/write

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5. (25 pts) Design a decoder to produce $\overline{BLOCK_SELECT}$ signals to enable memory and I/O devices to the following specifications:

16-bit address bus

The memory is to be addressed in 8 8K blocks in which

1 8K block is to be used for I/O

1 8K block is to be used for future I/O expansion.

1 8K block is to be used for ROM at high memory addresses.

1 8K block is to be used for future ROM expansion.

1 8K block is to be used for RAM at low memory addresses.

1 8K block is to be used for future RAM expansion.

Show how to use a 74LS138 decoder to generate the several $\overline{BLOCK_SELECT}$ signals.

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6. (25 pts) A 74LS138 decoder has the following address bits assigned to its inputs:

Address	74LS138 input
A7	A2
A6	A1
A5	A0
A4	E1
A3	E2
A2	E3
A1, A0	don't care

Assume an eight-bit address and make a table showing to what addresses each output responds.

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7. (40 pts) Design an input interface for a bank of 16 switches to be interfaced to an 8-bit data bus. Show how each switch is connected to be able to input a 1 or a 0. Assume the CPU has a separate I/O address space with an 8-bit I/O address and that the following control signals are available:

IO / \overline{M} 1 for I/O operations, 0 for memory access
 WR 1 for writing, 0 for not writing
 RD 1 for reading, 0 for not reading.

Use an 8-to-256 decoder with active-HIGH outputs in your design. (You do not need to use a real example of such a decoder. Just suppose you have such a thing to hand.)