

1. (10 pts)

- (a) (5 pts) T/F The MAX504 D/A converter expects serial data to be transferred MSB first.
- (b) (5 pts) T/F The Dallas Semiconductor DS1990A iButton expects serial data to be transferred MSB first.

2. (20 pts)

- (a) (10 pts) A certain device requires 450 ns to provide data to the 'C31. How many wait states must the 'C31 suffer through in order to accommodate this device? Assume the 'C31 is driven with a crystal clock with frequency $f_{XTAL} = 40 \text{ MHz}$.

$$f_{H_i} = \frac{f_{XTAL}}{2} = \frac{40 \text{ MHz}}{2} = 20 \text{ MHz} \quad T_{H_i} = \frac{1}{f_{H_i}} = \frac{1}{20 \text{ MHz}} = 50 \text{ ns}$$

$$\# \text{ of wait states} = \frac{\text{access time}}{T_{H_i}} - 1 = \frac{450 \text{ ns}}{50 \text{ ns}} - 1 = 8$$

- (b) (10 pts) How many wait states does the C31 insert when it accesses its internal RAM?

None

3. (20 pts) The following questions pertain to the Maxim MAX504 digital-to-analog converter.

- (a) (5 pts) What is the maximum gain error?

$$\pm 1 \text{ LSB}$$

- (b) (5 pts) To what extent can the reference voltage deviate from its nominal value? Give your answer in millivolts.

$$\pm 24 \text{ mV} \quad (T_A = 25^\circ \text{C}) \quad \text{OR} \quad \pm 37 \text{ mV} \quad (\text{MAX504B})$$
$$\text{OR} \quad \pm 33 \text{ mV} \quad (\text{MAX504C})$$

- (c) (5 pts) The figures in the datasheet showing how to connect the MAX504 in various configurations show a 33- μF capacitor from REFOUT to ground. What is the minimum permissible value of this capacitor?

$$3.3 \mu\text{F}$$

- (d) (5 pts) What is the maximum number of MAX504 devices which may be daisy-chained together?

Any number

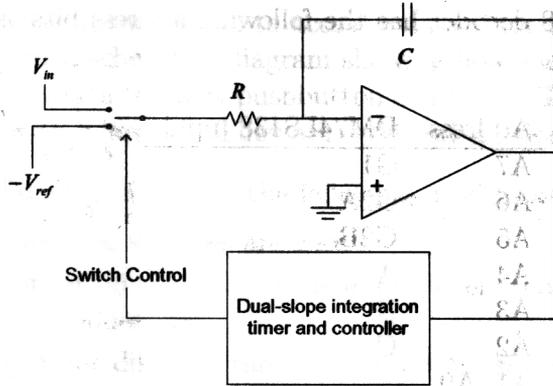


Figure 1: A Dual-Slope Integrator

4. (60 pts) A dual-slope integrator like the one in Figure 1 is required to handle input voltages between 0 V and +10 V. The designer has selected $V_{ref} = 10$ V.

(a) (30 pts) To achieve digital equivalents accurate to ± 1 mV, how many bits does the counter need? What is the maximum accuracy we could actually achieve from this choice?

Accuracy to ± 1 mV means steps are 2 mV wide.
 We need $\frac{10V}{2mV} = 5000$ steps.

To get this, we need $n = 13$ bits, or $2^n = 8192$ steps.
 A step is, then, $\frac{10V}{2^{13}} = 1.22$ mV, so the accuracy is

$$\pm \frac{1.22mV}{2} = \pm 610 \mu V$$

(b) (30 pts) To permit faithful representation of V_{in} in digital form, what is the highest frequency component V_{in} can contain? Assume that we clock the counter at a rate of $f_{clock} = 10$ MHz, meaning that the counter can be incremented or decremented at this rate, and that we run the counter from 0 to only 9,999 during the charging phase.

The longest integration time would occur for

$$V_{in} = 10V \quad T_{clock} = \frac{1}{f_{clock}} = \frac{1}{10MHz} = 100ns$$

we can count from 0 to 9,999 (10,000 cycles) in $(10000)(100ns) = 1ms$. the discharge of the capacitor would then also take 1ms, for 2ms in total!
 So 1 sample could take as long as 2ms.

we need at least 2 samples per period, so the signal period has to be at least $2(2ms) = 4ms$.
 So the signal frequency $f_{in} \leq \frac{1}{4ms} = 250$ Hz

5. (30 pts) A DM74LS138 decoder has the following address bits assigned to its inputs:

Address	DM74LS138 input
A7	G1
A6	G2A
A5	G2B
A4	A
A3	B
A2	C
A1, A0	—

Active high
} Active low

Assume addresses are eight-bits long and fill in the table below showing (in hexadecimal) the range of addresses which make each of the eight outputs go low.

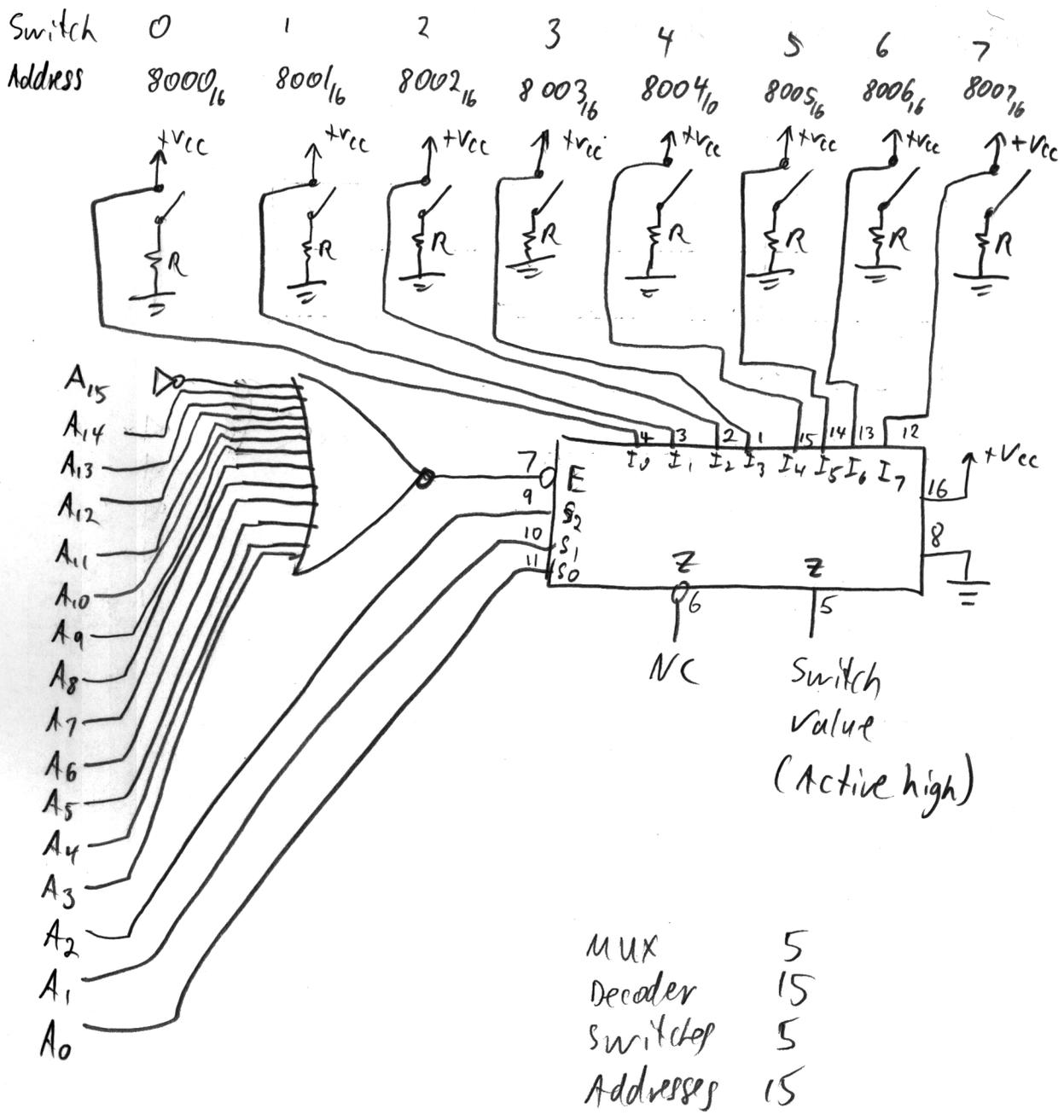
Output	Addresses which make it go low (0 V)
Y_0	$100000x_2 = 80_{16} \text{ to } 83_{16}$
Y_1	$100001x_2 = 84_{16} \text{ to } 87_{16}$
Y_2	$100010x_2 = 88_{16} \text{ to } 8B_{16}$
Y_3	$100011x_2 = 8C_{16} \text{ to } 8F_{16}$
Y_4	$100100x_2 = 90_{16} \text{ to } 93_{16}$
Y_5	$100101x_2 = 94_{16} \text{ to } 97_{16}$
Y_6	$100110x_2 = 98_{16} \text{ to } 9B_{16}$
Y_7	$100111x_2 = 9C_{16} \text{ to } 9F_{16}$

16:50
8:07
11:17

6. (60 pts) Use the world-wide web to access a data sheet for a 74AC151 8-input multiplexer. Draw a schematic diagram showing how such a multiplexer could be used in an interface to eight pushbutton switches. (These switches are not in an array, as with a keypad. They are eight independent switches.)

(a) (40 pts) Be sure to include the following in your solution:

- Show how the switches are wired.
- Account for *all* the pins on the multiplexer. If a pin is not used, mark it NC (no connection).
- Specify eight different ranges of 16-bit hexadecimal address to which this interface will respond, a separate range for each individual switch. Be sure your schematic shows the circuitry necessary to decode these addresses and activate the interface. Use only AND, OR, and NOT gates (and possibly the multiplexer itself) in the decoder.



(b) (20 pts) Assuming each of the gates has a propagation delay of 5 ns, estimate the access time of this interface. This is the time elapsed after the address lines are stable until data are available on the data bus for the 'C31 to read. Be sure to consider the delay of the multiplexer in arriving at your answer. Assume the temperature will not exceed 35 °C and also assume $V_{CC} = 5$ V.

The delay in the decoder is 10 ns (5 ns for the inverter, 5 ns for the 13-input NOR gate.)

The delay for the multiplexer is at most 15 ns, so the total delay is at most

$$10 \text{ ns} + 15 \text{ ns} = 25 \text{ ns}.$$