Practical Issues in Implementing Analog-to-Information Converters

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***Abstract*— The stability and programmability of digital signal processing systems has motivated engineers to move the analog-to-digital conversion (ADC) process closer and closer to the front end of many signal processing systems in order to perform as much processing as possible in the digital domain. Unfortunately, many important applications, including radar and communication systems, involve wideband signals that seriously stress modern ADCs; sampling these signals above the Nyquist rate is in some cases challenging and in others impossible. While wideband signals by definition have a large bandwidth, often the amount of information they carry per second is much lower; that is, they are *compressible* in some sense. The first contribution of this paper is a new framework for wideband signal acquisition purpose-built for compressible signals that enables sub-Nyquist data acquisition via an *analog-to-information converter* (AIC). The framework is based on the recently developed theory of *compressive sensing* in which a small number of non-adaptive, randomized measurements are sufficient to reconstruct compressible signals. The second contribution of this paper is an AIC implementation design and study of the tradeoffs and non-idealities introduced by real hardware. The goal is to identify and optimize the parameters that dominate the overall system performance.**

I. Introduction

The prevalence of digital signal processing in communication applications has popularized the use the analog-to-digital converters (ADC). These ADCs employ the Nyquist sampling theorem which guarantees the reconstruction of a band-limited signal when it is uniformly sampled with a rate of at least twice its bandwidth. Accordingly, an exceedingly large number of samples is needed to represent wideband signals, requiring large amounts of resources for storing and transmitting such data. Emerging applications like radar detection and ultra-wideband communication are pushing the performance of ADCs toward their physical limits.

In many cases of interest the signals have additional structure than band-limitedness alone. Over the past two years, a new theory of *compressive sensing* (CS) has emerged, which exploits this knowledge to achieve signal reconstruction using fewer measurements than the number prescribed by the Nyquist theorem for certain classes of signals. In particular, CS allows reconstruction of signals which are compressible by some transform, meaning that the transform representation has a few large coefficients and many small coefficients. As an example, signals that have smooth variations are compressed by the Fourier transform, while signals with localized variations are compressed by the wavelet transform. By leveraging the CS theory, an analog-to-information converter (AIC) can be designed to acquire samples at a lower rate while successfully recovering the compressible signal of interest.

In this paper, we develop an AIC system that leverages the CS theory while addressing practical considerations that arise in an actual hardware implementation. We first extend the existing CS framework to analog signals. We also study the effects of non-idealities on the performance of the AIC system, which mirror the same behaviors of traditional ADCs. We find that it is possible to obtain the same performance regarding Signal to Noise Ratio (SNR) or Effective Number of Bits (ENOB) while sampling with a rate that is much lower than the Nyquist rate.

Our models for non-idealities enable the evaluation of performance and feasibility of various AIC hardware implementations. In addition, we provide behavioral models for circuit simulation that reduce the duration of the development process, while maintaining accurate performance predictions.

This paper is organized as follows. First, we provide an overview of theory and algorithms for CS and extend the mathematical framework to AICs in Section II. We then conduct a number of experiments to validate our approach in Section III and we conclude in Section IV.

II. Compressive Sensing for AIC Systems

A. Compressive sensing background

Compressive Sensing (CS) provides a framework for acquisition of an $N \times 1$ discrete-time signal vector $\mathbf{x} = \boldsymbol{\Psi}\boldsymbol{\alpha}$ that is K-*sparse* or *compressible* in some *sparsity basis* matrix $\boldsymbol{\Psi}$ (where each column is a basis vector ψ_i). By K-sparse we mean that $\|\boldsymbol{\alpha}\|_0 = K \ll N$, where $\|\cdot\|_0$ denotes the ℓ_0 norm, which counts number of nonzero coefficients in the vector $\boldsymbol{\alpha}$. By compressible we mean that the entries of $\boldsymbol{\alpha}$, when sorted from largest to smallest, decay rapidly to zero; such a signal is well approximated using a K-term representation.

The CS framework, first introduced by Candès, Romberg, and Tao [1] and Donoho [2], demonstrates that a signal that is K-sparse or compressible in one basis $\boldsymbol{\Psi}$ can be recovered from $M = cK$ *nonadaptive* linear projections onto a second basis $\boldsymbol{\Phi}$ that is *incoherent* with the first, where c is a small *overmeasuring* constant. By incoherent, we mean that the rows ϕ_j of the matrix $\boldsymbol{\Phi}$ cannot sparsely represent the elements of

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the sparsity-inducing basis ψ_i, and vice versa [1], [2]. Thus, rather than measuring the N-point signal $\mathbf{x}$ directly, we acquire the $M \ll N$ linear projections $\mathbf{y} = \mathbf{\Phi x} = \mathbf{\Phi \Psi \alpha}$. For brevity, define the $M \times N$ matrix $\mathbf{\Theta} = \mathbf{\Phi \Psi}$.

Most of the CS literature focuses on the case where the elements of $\mathbf{\Phi}$ are independently drawn from a random distribution. This construction provides the additional property of *universality* meaning that compressible signals can be reconstructed from these random measurements regardless of the signal's structure. Additionally, this measurement scheme has been successfully implemented using psuedo-random number generators.

Since $M < N$, recovery of the signal $\mathbf{x}$ from the measurements $\mathbf{y}$ is ill-posed in general; however, the additional assumption of signal *sparsity* or *compressibility* in the basis $\mathbf{\Psi}$ makes recovery both feasible and practical. The recovery of the sparse set of significant coefficients $\boldsymbol{\alpha}$ can be achieved through *optimization* by searching for the signal with the smallest ℓ_0 norm for the coefficient vector $\boldsymbol{\alpha}$ that agrees with the M observed measurements in $\mathbf{y}$. While solving this ℓ_0 optimization problem is prohibitively complex (it is believed to be NP-hard [3]), if we use $M = O(K \log(N/K))$ measurements, then we need only solve for the coefficient vector $\boldsymbol{\alpha} = [\alpha_1, \alpha_2, \ldots, \alpha_N]$ with the smallest ℓ_1 norm that agree with the measurements $\mathbf{y}$ [1], [2]

$$\widehat{\boldsymbol{\alpha}} = \arg\min \|\boldsymbol{\alpha}\|_1 \quad \text{s.t. } \mathbf{y} = \mathbf{\Phi \Psi \alpha}. \tag{1}$$

This optimization problem, also known as *Basis Pursuit* [4] can be solved with traditional linear programming techniques whose computational complexities are polynomial in N. At the expense of slightly more measurements, iterative greedy algorithms like Orthogonal Matching Pursuit (OMP) [5] can also be applied to the recovery problem.

B. AIC: Signal processing issues

Several issues need to be resolved in order to apply the CS framework to our case of interest. First, the concept of compressibility has been developed only in the context of discrete signals. Second, the multiplication process with a dense measurement matrix is not feasible in hardware for streaming signals. Finally, we require a setup to obtain a discrete set of measurements from from a continuous signal. Considering these issues, we now extend the CS framework to continuous signals in order to build a new family of sampling devices.

1) Analog signal model: We develop a model for representing analog signals that uses a finite number of parameters per unit time in some dictionary of continuous functions. Let the analog signal $x(t), t \in [0, T]$ be composed of a *finite* number of weighted continuous dictionary components

$$x(t) = \sum_{n=1}^{N} \alpha_n \, \psi_n(t), \tag{2}$$

with $\alpha_n \in \mathbb{R}$ for some signal length T. In cases where there are a small number of entries with large magnitudes in $\boldsymbol{\alpha}$, we may again say that the signal x is "compressible". Although each of the dictionary elements ψ_n may have high bandwidth, the signal itself has relatively few degrees of freedom. Ideally, we would like to sample the signal at some multiple of the number of degrees of freedom, rather than at twice the bandwidth as required by the Shannon/Nyquist sampling theorem.

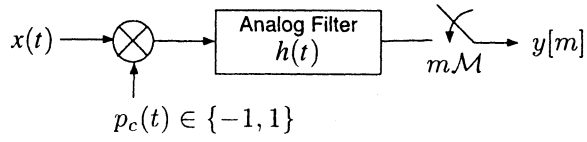

Figure 1. Pseudo-random demodulation scheme for AIC.

2) Analog processing: Our signal acquisition system consists of three main components; demodulation, filtering, and uniform sampling. As seen in Figure 1, the signal is modulated by a psuedo-random maximal-length PN sequence of ± 1's. We call this the *chipping sequence* $p_c(t)$; its chipping rate, i.e. the rate of change of symbols, must be faster than the Nyquist rate for the input signal. The purpose of such modulation is to provide randomness necessary for successful CS recovery. The modulation is followed by a low-pass filter with impulse response $h(t)$. Finally, the signal is sampled at rate $\mathcal{M}$ using a traditional ADC.

3) Analog system as a CS matrix: The discrete measurement vector $\mathbf{y}$ can be characterized as a linear transformation of the discrete coefficient vector $\boldsymbol{\alpha}$. As in the discrete CS framework, we can express this transformation as an $M \times N$ matrix $\mathbf{\Theta}$ that combines two processes: the signal synthesis operator $\mathbf{\Psi}$, which maps the discrete coefficient vector $\boldsymbol{\alpha}$ to an analog signal $x(t)$, and the signal measurement operator $\mathbf{\Phi}$, which maps the analog signal $x(t)$ to the discrete set of measurements $\mathbf{y}$.

To find the matrix $\mathbf{\Theta}$ we start by considering the output $y[m]$, which is a result of convolution and demodulation followed by sampling at rate $\mathcal{M}$

$$y[m] = \int_{-\infty}^{\infty} x(\tau)\, p_c(\tau)\, h(t-\tau)\, d\tau \Big|_{t=m\mathcal{M}}. \tag{3}$$

Our analog input signal (2) is composed of a finite and discrete number of components of $\mathbf{\Psi}$, and so we can expand (3) to

$$y[m] = \sum_{n=1}^{N} \alpha_n \int_{-\infty}^{\infty} \psi_n(\tau)\, p_c(\tau)\, h(m\mathcal{M} - \tau)\, d\tau. \tag{4}$$

It is now clear that we can separate out an expression for each element $\theta_{m,n} \in \mathbf{\Theta}$ for row m and column n

$$\theta_{m,n} = \int_{-\infty}^{\infty} \psi_n(\tau)\, p_c(\tau)\, h(m\mathcal{M} - \tau)\, d\tau. \tag{5}$$

to obtain an equivalent representation $\mathbf{y} = \mathbf{\Theta \alpha}$.

C. Reconstruction for Time-Frequency Signals

Signals used in communication schemes are known to be time-frequency sparse since they often consist of bandlimited

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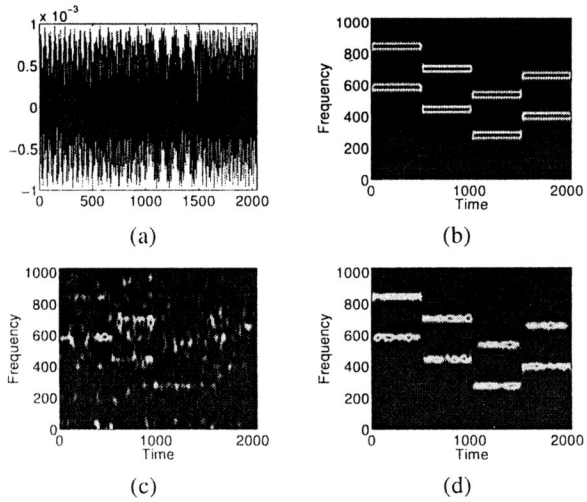

Figure 2. Comparison of Fourier vs. Gabor reconstruction from measurements taken at 25% of Nyquist rate. (a) Fourier sparse signal modulated by different frequencies over time. (b) Spectrogram of the signal. (c) Spectrogram of CS-based reconstruction of the signal using a Fourier basis. (d) Spectrogram of CS-based reconstruction of the signal using a Gabor dictionary.

signals which are modulated using different frequencies at different times, as is the case in frequency hopping radios [6], where signals are modulated by a signal with rapidly-changing frequency to avoid jamming or detection. A classical analysis tool for this class of signals is a *spectrogram*. A spectrogram is assembled using the magnitude of short-time Fourier transforms (STFT) that performs Fourier analysis of windowed versions of the input signals to establish frequency content at local time neighborhoods. The STFT is written as

$$\alpha(t,f) = \langle x, \psi_{\tau,f} \rangle = \int_{-\infty}^{\infty} x(t) g(t-\tau) e^{-j2\pi f t} dt$$

where g is a window with $\|g\|_2 = 1$. This formulation allows us to track changes in frequency over time. More importantly, we can build a dictionary of such local time-frequency atoms (such as Gabor atoms) that sparsifies a signal that features dynamic frequency content over time. Thus, by using such a dictionary during CS reconstruction we obtain a spectrogram as the resulting representation.

Figure 2(a) shows a Fourier sparse signal which has been sinusoidally modulated with different frequencies over four sections of time. The spectrogram of this signal is also displayed in Figure 2(b). We see that for small ranges of time, the signal is very sparse in the frequency domain, but when we consider the whole signal length the frequency content becomes diffused.

We show two examples of reconstruction from the random demodulation system. The first reconstruction, for a signal with spectrogram shown in Figure 2(c), uses the Fourier basis as the sparse dictionary and operated on a measurement rate equal to 25% of the Shannon Theorem required sampling rate. The spectrogram pictured in Figure 2(d) shows reconstruction of the same measurements using a Gabor dictionary with a

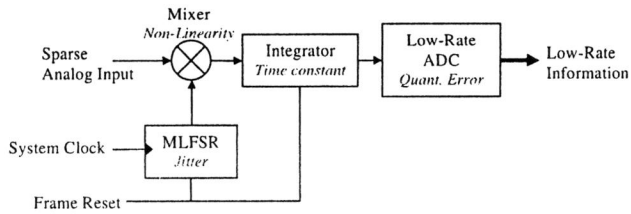

Figure 3. System block diagram.

boxcar window. The active frequencies are much more apparent with the Gabor dictionary since we are taking advantage of the time localization.

III. Implementation Issues and Behavioral Modeling

Circuit implementation of system-level components results in non-ideal behaviors and often degrades the system performance. These unavoidable non-ideal behaviors must be considered during the design and performance analysis of the AIC since the actual performance metrics will deviate from the expected values. In this section, we study the dominant non-idealities inherent to the four main system-level blocks (shown in Figure 3); the pseudo-random number generator, integrator (low pass filter), quantizer and mixer (multiplier). To analyze the effect of non-ideal blocks on the overall system performance, we treat only one block as non-ideal at a time for each type of non-ideality. This allows us to judge the sensitivity of the overall system performance to the varying degrees of non-ideality of the different parameters and identify the dominant parameters that need to be carefully considered during the physical design of the AIC's. To facilitate faster design-space exploration without using a time consuming circuit simulation technique, we present efficient methods for behavioral modeling of the different blocks.

A. Behavioral Models

Ideal system level models are insufficient for hardware design because they do not model real behavior of hardware components. Traditionally, the real behavior of components is modeled with time consuming circuit level simulations. In order to decrease design time, we demonstrate *behavioral models* which produce the same results as the costly circuit models, but reduce the complexity of simulation. With such time-efficient models, we can explore the design space and invoke automated synthesis and optimization routines to simplify the design process. With our simulations, we examine the quality of these models and provide evidence that they correctly estimate the performance of the real system.

Figure 4 shows end to end simulation of an example signal composed of two frequencies (10MHz and 20MHz) together with the reconstructed signal. Reconstruction results prove that the measurement at rates of 10 MSamples/s ($\frac{1}{4}$ of Nyquist rate) is faithfully able to reconstruct the signal with a small amount of added noise (spurious free dynamic range = 65 dB). This

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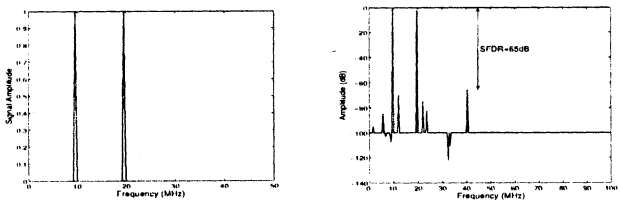

(a) (b)

Figure 4. (a) Example two tone input signal at 10 MHz and 20 MHz. (b)SFDR for a dual tone signal AICed at 10 MSample/s.

demonstrates that the system still performs reasonably well in substantial amounts of additive noise. In the following, we are going to present the different non-idealities that arise form the practical hardware implementation and show their effects on the output signals accuracy.

B. Pseudo-Random Number Generator (RNG)

The pseudo-random number generator (RNG, also known as a feedback shift register) is a digital block that is composed of flip-flops and XOR gates and generates PN-sequences of a given length. The most important non-ideality in this block is the *jitter* effect that occurs when a clock edge arrives before or after its expected time. The time variation t_j, is called the *aperture time jitter*. Uncertainty in the clock edge degrades the overall system SNR according to:

$$\mathrm{SNR(dB)} = 20\ \log\left(\frac{1}{2\pi f t_j}\right) \tag{6}$$

where f is the input signal frequency (assuming a sine wave) and t_j is the aperture time jitter. The results of this degradation can be seen in Figure 5. Spurious free dynamic range (SFDR) is the ratio of the RMS value of the signal to the RMS value of the worst spurious signal, regardless of where it falls in the frequency spectrum. The largest magnitude spur is not necessarily a harmonic of the original signal. SFDR is an important specification in communications systems because it represents the smallest value of signal that can be distinguished from a large interfering signal, also known as a blocker.

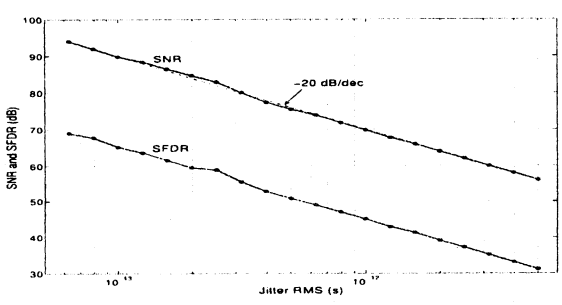

Figure 5. Simulation of the overall system performance in terms of SNR and SFDR by changing jitter effect value.

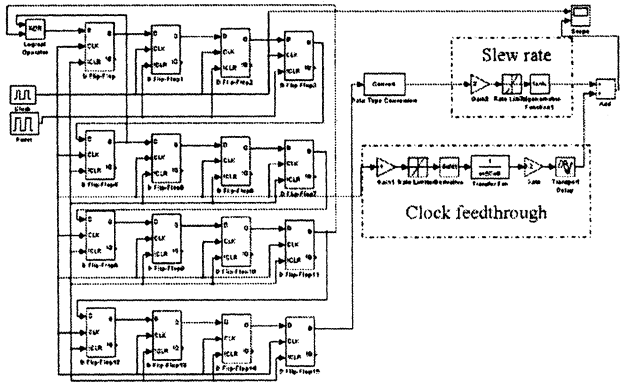

Figure 6. Behavioral model of the 16-bit SDFF random number generator.

For generating high speed pseudo-random binary sequences, it is important to choose high speed components. The Semi Dynamic Flip Flop (SDFF) proposed in [7] was shown to be the fastest DFF in comparison to other existing architectures. The SDFF is the most convenient structure for applications where speed is of primary importance, and yet does not induce a big penalty in terms of power consumption. In Figure 6 we present a behavioral model of the pseudo-random number generator that includes all the different non-idealities inherent in a circuit implementation of an SDFF. The different blocks in the model are: an ideal 16-bit RNG, clock feedthrough block and the block for varying the slew rate.

C. Quantizer

The quantizer block converts each sample from an analog voltage to a digital value and approximates every sample to the nearest digital value, although with some quantization error that limits the SNR according to the equation:

$$\mathrm{SNR(dB)} = 6.02N + 1.76 \tag{7}$$

where N is the number of bits required for appropriately representing the digital signal. The above equation shows that the SNR of the converted signal is increases by approximately 6 dB for each additional bit of the converted digital data, meaning that better performance will be obtained by increasing the number of quantizer bits. For the quantizer used in this work, simulation results for the SNR vs. the number of bits is shown in Figure 7, which approximately follow the trend predicted by Equation 7.

D. Integrator

The integrator used in our work can be implemented in different ways, for instance, the active-RC implementation depicted in Figure 8(a). The integration equation for this implementation can be derived as:

$$\frac{V_{out}}{V_{in}} = \frac{\frac{-A_o}{(A_o+1)R_1C}}{s + \frac{1}{R_2C} + \frac{1}{(A_o+1)R_1C}} \tag{8}$$

where A_o is the finite op-amp gain, R_1, R_2 and C are the passive element values. The ideal and actual behaviors of such

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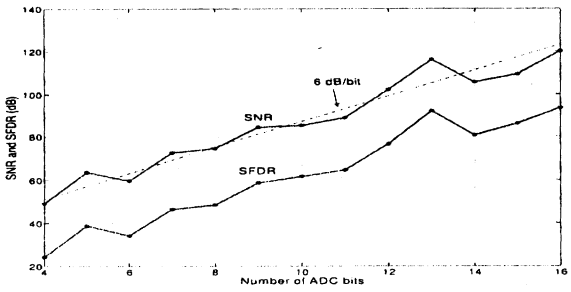

Figure 7. Simulation of the overall system performance in terms of SNR and SFDR by changing number of quantizer bits.

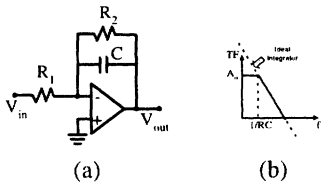

Figure 8. (a) Integrator active-RC implementation. (b)The actual and ideal integrator performance (TF vs. frequency).

a circuit are represented in Figure 8(b). It is apparent from the transfer function that an ideal integrator $(1/s)$ cannot be achieved in practice since an infinite gain cannot be obtained at DC level (s=0). Therefore, any implementation of an integrator can be interpreted as a low pass filter $(1/(s+a))$ because of the finite gain of the circuits. Performance (SNR) is increasingly degraded with the constant a as shown in Figure 9.

E. Mixer (Multiplier)

Modulators, also known as mixers, compute $x(t) \times m(t)$, where m(t) may include sinusoids, chirps, sequences of ± 1's, etc., for each signal $x(t)$. Passive mixers, such as diode mixers and passive field effect transistor (FET) mixers, have good linearity, good noise performance, and can operate at frequencies up to 5GHz [8]. However, active mixers are preferred for low-power integrated circuits as they provide

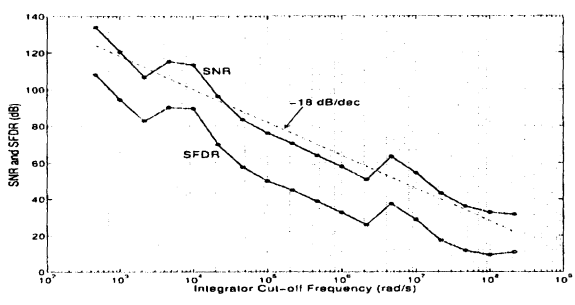

Figure 9. Simulation of the overall system performance in terms of SNR and SFDR by changing integrator's cutoff frequency value.

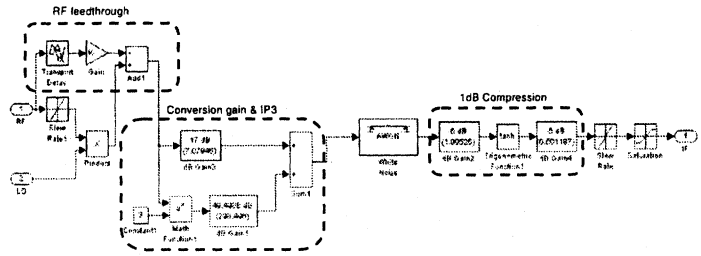

Figure 10. Behavioral model of Gilbert-cell based active mixer.

high conversion gain, require less power at the local input port, and have a broader design space. Mixers are generally based on the classic Gilbert cell [9]. Several modifications can be made to this basic circuit to enhance its frequency response, decrease its nonlinearity, and limit its noise level. The most important non-ideality inherent to the actual circuit implementation for the mixer is the non-linearity. The linearity of the mixer is measured using two parameters: the 1dB compression point also known as input compression point (ICP) and the third harmonic input intercept point (IIP3 or simply IP3). The ICP gives the value of the input RF power at which the gain drops 1 dB below its value in the linear operation range. The IP3 of the mixer represents the input RF power at which the output 3rd harmonic components will equal the fundamental component. Ideally, there should be zero 3rd order harmonics in the output when the transfer function is perfectly linear making the IP3 located at infinity. However, due to the nonlinear transfer function of the mixer, the 3rd harmonic components are present in the mixer output and the IP3 has a finite value.

In Figure 10, we present the behavioral model of the mixer that includes all the non-idealities present in the circuit implementation of the mixer. This model includes the ideal multiplication, RF port feedthrough, conversion gain, IIP3, output referred noise, 1dB compression, maximum frequency

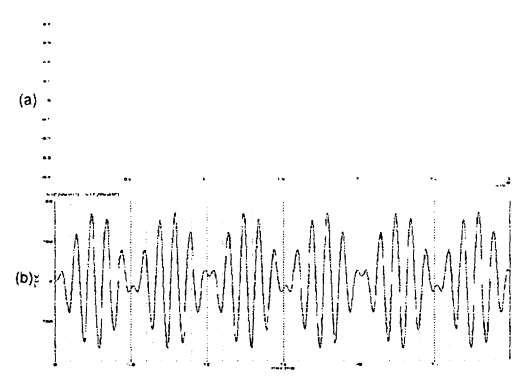

Figure 11. (a)The waveform generated from our model for the mixer. (b)The waveform generated from the simulation of the actual circuit implementation for the mixer.

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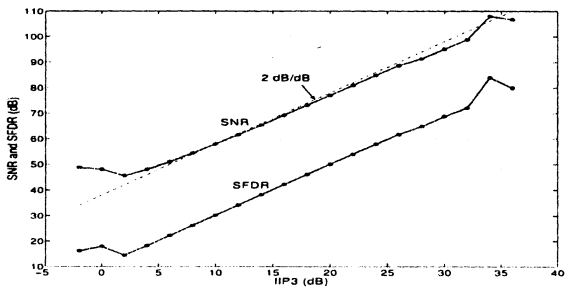

Figure 12. Simulation of the overall system performance in terms of SNR and SFDR by changing mixer linearity by changing the IP3 value.

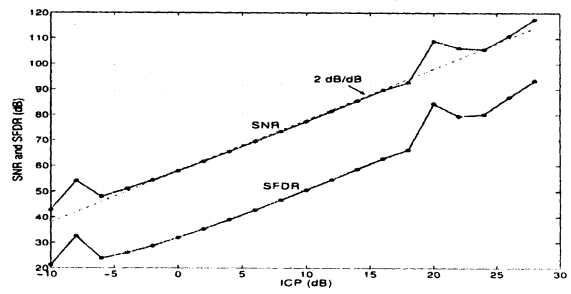

Figure 13. Simulation of the overall system performance in terms of SNR and SFDR by changing mixer linearity by changing the ICP value.

limitation, and saturation of the output at the values of the upper and lower supply voltages. The output waveform from the non-ideal mixer model is shown in Figure 11(a), while the simulation result of the mixer circuit using Cadence Spectre [10] is shown in Figure 11(b). Comparing the two plots, we see that the developed model faithfully represents the circuit behavior.

To measure the impact of the linearity of the mixer on the overall system performance, we measured the system performance, represented by SNR and SFDR (sparse free dynamic range), under varying degrees of linearity. We also studied the individual impact of the IP3 and the ICP on the overall system performance to determine their relative effectiveness in terms of introducing non-ideality in the circuit. The simulation results from our behavior model for the impact of IP3 on the overall system performance is shown in Figure 12 while the simulation results for the impact of ICP on the overall system performance is shown in Figure 13. From these simulations, we notice that as the linearity enhances in terms of either IP3 or ICP, the overall system performance is enhanced in terms of SNR or SFDR. While the slope of improvement is the same, the IP3 effect is slightly more dominant than the ICP effect in system overall performance. Therefore, the designers need to consider mixer linearity as the dominant design parameters for the mixer in terms of both IP3 and ICP but have to give more care for IP3.

From the simulation results, it is apparent that the mixer non-linearity is more dominant in determining the overall performance of the system as compared to the effects of clock jitter and the non-ideality of the integrator. The quantizer error cannot be compared to the other sources of errors since the quantizer error can be improved by increasing the number of bits. However, extra hardware is required for increasing the number of bits apart from the associated implementation difficulties, if any. We also note that the impact of the clock jitter and integrator non-idealities are very similar, although enhancing the integrator performance is much easier than reducing the clock jitter. Therefore, for enhancing system performance by reducing component level non-idealities, we recommend the following enhancements in the order of preference: enhancing the mixer linearity, increasing the number of quantization bits, enhancing the integrator performance and improving the clock jitter.

IV. Conclusion

In this paper, we have developed both new theory and an implementation for AIC of wideband signals. Our new theory bridges the gap between the current CS theory, which is based on discrete-time signals, and the needs of real data acquisition devices, which deal with continuous-time signals. Our behavioral models have enabled us to study the design space for the four key building blocks in order to optimize the end-to-end performance. Our study of the non-idealities introduced by actual circuit implementations suggests that the mixer non-linearity dominates over the effects of clock jitter in the chipping sequence generator and the non-ideal transfer function of the integrator. We thus recommend the following enhancements in order of expected performance impact: enhancing the mixer linearity, increasing the number of quantization bits, enhancing the integrator performance, and improving the clock jitter.

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