Multicycle Approach

• Break up the instructions into steps, each step takes a cycle
  – balance the amount of work to be done
  – restrict each cycle to use only one major functional unit:

• At the end of a cycle
  – store values for use in later cycles
  – introduce additional “internal” registers

• Each instruction will take _________ cycles to fully execute
Simplified Multicycle Datapath

Breaking down an instruction

• Steps for an R-type instruction:
  - IR <= Memory[PC]
  - A <= Reg[IR[25:21]]
  - B <= Reg[IR[20:16]]
  - ALUOut <= A op B
  - Reg[IR[15:11]] <= ALUOut

• What did we forget?

• Above notation is called RTL – Register Transfer Language
Example #1 – sub $t0, $s1, $s2

1. IR <= Memory[PC]
2. A <= Reg[IR[25:21]]
3. B <= Reg[IR[20:16]]
4. ALUOut <= A op B
5. Reg[IR[15:11]] <= ALUOut
6. PC <= PC + 4

Example #2 – lw $t0, 8($s2)

1. IR <= Memory[PC]
2. A <= Reg[IR[25:21]]
3. ALUOut <= A + sign-extend(IR[15-0])
4. MDR = Memory[ALUOut]
5. Reg[IR[20-16]] = MDR
6. PC <= PC + 4
How many cycles do we need?

In once cycle can do: Register read or write, memory access, ALU

a.) Fill in the cycle number for each task below

<table>
<thead>
<tr>
<th>Cycle #</th>
<th>Task (for R-type instruction)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>IR &lt;= Memory[PC]</td>
</tr>
<tr>
<td></td>
<td>A &lt;= Reg[IR[25:21]]</td>
</tr>
<tr>
<td></td>
<td>B &lt;= Reg[IR[20:16]]</td>
</tr>
<tr>
<td></td>
<td>ALUOut &lt;= A op B</td>
</tr>
<tr>
<td></td>
<td>Reg[IR[15:11]] &lt;= ALUOut</td>
</tr>
<tr>
<td></td>
<td>PC &lt;= PC + 4</td>
</tr>
</tbody>
</table>

b.) What is the total number of cycles needed?

Multicycle Implementation

- Goals:
  - Pack as much work into each step as possible
  - Share steps across different instruction types

- 5 Steps
  1. Instruction Fetch
  2. Instruction Decode and Register Fetch
  3. Execution, Memory Address Computation, or Branch Completion
  4. Memory Access or R-type instruction completion
  5. Write-back step
Step 1: Instruction Fetch

IR <= Memory[PC];
PC <= PC + 4;

What is the advantage of updating the PC now?

Step 2: Instruction Decode and Register Fetch

- Read registers rs and rt
  A <= Reg[IR[25:21]];
  B <= Reg[IR[20:16]];

- Compute the branch address
  ALUOut <= PC + (sign-extend(IR[15:0]) << 2);

- Does this depend on the instruction type?

- Could it depend on the instruction type?
Step 3 (instruction dependent)

- ALU function depends on instruction type
  1. ________________
     \[ \text{ALUOut} \triangleq A + \text{sign-extend}(\text{IR}[15:0]) \; \]
  2. ________________
     \[ \text{ALUOut} \triangleq A \text{ op B} \; \]
  3. ________________
     \[ \text{if} \; (A==B) \; \text{PC} \triangleq \text{ALUOut} \; \]

Step 4 (R-type or memory-access)

- Loads and stores access memory
  \[ \text{MDR} \triangleq \text{Memory}[\text{ALUOut}] ; \]
  or
  \[ \text{Memory}[\text{ALUOut}] \triangleq B ; \]
- R-type instructions finish
  \[ \text{Reg}[\text{IR}[15:11]] \triangleq \text{ALUOut} ; \]

*The write actually takes place at the end of the cycle on the edge*
Step 5: Write-back

- $\text{Reg}[\text{IR}[20:16]] \leftarrow \text{MDR};$

Which instruction needs this?

Summary:

<table>
<thead>
<tr>
<th>Step name</th>
<th>Action for RTtype instructions</th>
<th>Action for memory-reference Instructions</th>
<th>Action for branches</th>
<th>Action for jumps</th>
</tr>
</thead>
<tbody>
<tr>
<td>Instruction fetch</td>
<td>$R \leftarrow \text{Memory}(\text{PC})$</td>
<td>$\text{PC} \leftarrow \text{PC} + 4$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Instruction decode/registers fetch</td>
<td>$A \leftarrow \text{Reg}[\text{IR}[20:16]]$</td>
<td>$B \leftarrow \text{Reg}[\text{IR}[20:16]]$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$\text{ALUOut} \leftarrow \text{PC} + \text{signextend}(\text{PELS}[0:0]) \ll 2$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Execution, address computation, branch/jump completion</td>
<td>$\text{ALUOut} \leftarrow A \oplus B$</td>
<td>$\text{ALUOut} \leftarrow A \oplus \text{signextend}(\text{IR}[15:0])$</td>
<td>$\text{PC} \leftarrow \text{ALUOut}$</td>
<td>$\text{PC} \leftarrow \text{IR}[31:20]$, $\text{IR}[25:0], \text{PELS}[0:0]$</td>
</tr>
<tr>
<td>Memory access or result completion</td>
<td>$\text{Reg}[\text{IR}[15:11]] \leftarrow \text{ALUOut}$</td>
<td>$\text{Load MDR} \leftarrow \text{Memory(\text{ALUOut})}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>or $\text{Store Memory(\text{ALUOut})} \leftarrow B$</td>
<td>or $\text{Store Memory(\text{ALUOut})} \leftarrow B$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Memory read completion</td>
<td>$\text{Load Reg}[\text{IR}[20:16]] \leftarrow \text{MDR}$</td>
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</tbody>
</table>

**Figure 5.20** Summary of the steps taken to execute any instruction class. Instructions take from three to five execution steps. The first two steps are independent of the instruction class. After these steps, an instruction takes one to three more cycles to complete, depending on the instruction class. The empty entries for the Memory access step or the Memory read completion step indicate that the particular instruction class takes fewer cycles. In a multicycle implementation, a new instruction will be started as soon as the current instruction completes, so these cycles are not idle or wasted. As mentioned earlier, the register file actually reads every cycle, but as long as the IR does not change, the values read from the register file are identical. In particular, the value read into register B during the Instruction decode stage, for a branch or RTtype instruction, is the same as the value stored into B during the Execution stage and then used in the Memory access stage for a store-word instruction.
Questions

• How many cycles will it take to execute this code?

```assembly
lw $t2, 0($t3)
lw $t3, 4($t3)
beq $t2, $t3, Label  #assume not taken
add $t5, $t2, $t3
sw $t5, 8($t3)
Label: ...
```

• What is going on during the 8th cycle of execution?

• In what cycle does the actual addition of $t2$ and $t3$ take place?

Control for Multicycle Implementation
Control for “sub $t0, $s1, $s2”
ALUSrcA =
ALUSrcB =

Multicycle Control

- Control for single cycle implementation was ______________, based only on the ___________
- Control for multicycle implementation will be ______________, based on the __________ and current ___________
- We’ll implement this control with state machines
Two Weird Things

1. For enable signals (RegWrite, MemRead, etc.) we’ll write down the signal only if it is true. For multiplexors (ALUSrcA, IorD, etc.) we’ll always say what the value is. (unless it’s a “don’t care”)

2. Some registers are written every cycle, so no write enable control for them (MDR, ALUOut). Others have explicit control (register file, IR)

Random (but useful) Refresher:
- ALUOp = 00 → ALU adds
- ALUOp = 01 → ALU subtracts
- ALUOp = 10 → ALU uses function field

Example Control

Step 1: Instruction Fetch
- IR <= Memory[PC]
- PC <= PC + 4
Step 2: Decode/Register Fetch

A <= Reg[IR[25:21]];
B <= Reg[IR[20:16]];
ALUOut <= PC + (sign-extend(IR[15:0]) << 2);

FSM for Multicycle Control

- How many state bits will we need?
Finite State Machine for Control

- Implementation:

Chapter 5 Summary

- If we understand the instructions...
  We can build a simple processor!
- If instructions take different amounts of time, multi-cycle is better
- Datapath implemented using:
  - Combinational logic for arithmetic
  - State holding elements to remember bits
- Control implemented using:
  - Combinational logic for single-cycle implementation
  - Finite state machine for multi-cycle implementation